Nos. 2024-1312, 2024-1313

United States Court of Appeals for the Federal Circuit

MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., MICRON TECHNOLOGY TEXAS, LLC,
Appellants,

v.

NETLIST, INC.,
Appellee.

Appeal from the United States Patent and Trademark Office,
Patent Trial and Appeal Board, in No. IPR2022-00744, IPR2022-00745

CORRECTED BRIEF OF APPELLANTS

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PATENT CLAIMS AT ISSUE

U.S. Patent No. 10,489,314

1. A memory module operable in a computer system to communicate data with a memory controller of the computer system at a specified data rate via a N-bit wide data bus in response to memory commands received from the memory controller, the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first burst of N-bit wide data signals and a first burst of data strobes and the second memory command to cause the memory module to receive or output a second burst of N-bit wide data signals and a second burst of data strobes, the memory module comprising:

    a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

    a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, wherein the plurality of N-bit wide ranks include a first rank configured to receive or output the first burst of N-bit wide data signals and the first burst of data strobes at the specified data rate in response to the first memory command, and a second rank configured to receive or output the second burst of N-bit wide data signals and the second burst of data strobes at the specified data rate in response to the second memory command;

    circuitry coupled between the plurality of N-bit wide ranks and the N-bit wide data bus; and

    logic coupled to the circuitry and configured to respond to the first memory command by providing first control signals to the circuitry and to subsequently respond to the second memory command by providing second control signals to the circuitry, wherein the circuitry is configured to enable data transfers through the circuitry in response to the first control signals and subsequently in response to the second control signals, wherein respective N-bit wide data signals of the first burst of N-bit wide data signals and respective data strobes of the first burst of data strobes are transferred at the specified data rate between the first rank and the N-bit wide data bus through the circuitry, and wherein respective N-bit wide data

signals of the second burst of N-bit wide data signals and respective data strobes of the second burst of data strobes are transferred at the specified data rate between the second rank and the N-bit wide data bus through the circuitry;

wherein the data transfers through the circuitry are registered data transfers enabled in accordance with an overall CAS latency of the memory module, and the circuitry is configured to add a predetermined amount of time delay for each registered data transfer through the circuitry so that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the plurality of memory integrated circuits.

15. A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

logic coupled to the printed circuit board and configured to receive a first set of input address and control signals associated with a first read or write memory command and to output a first set of registered address and control signals in response to the first set of input address and control signals, the first set of input address and control signals including a first plurality of input chip select signals, the first set of registered address and control signals including a first plurality of registered chip select signals corresponding to respective ones of the first plurality of input chip select signals, the first plurality of registered chip select signals including a first registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value;

memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, wherein the plurality of N-bit wide ranks are configured to receive respective ones of the first plurality of registered chip select signals, wherein a first N-bit wide rank in the plurality of N-bit wide ranks receiving the first registered chip select signal having the active signal value is configured to receive or output a first burst of N-bit wide data

signals and a first burst of data strobes associated with the first read or write command;

circuitry coupled between data and strobe signal lines in the N-bit wide memory bus and corresponding data and strobe pins of memory devices in each of the plurality of N-bit wide ranks; and

wherein the logic is further configured to, in response to the first read or write memory command, output first control signals to the circuitry, and wherein the circuitry is configured to enable data transfers between the first rank and the memory bus through the circuitry in response to the first control signals so that respective N-bit wide data signals of the first burst of N-bit wide data signals and respective data strobes of the first burst of data strobes are transferred through the circuitry in accordance with an overall CAS latency of the memory module; and

wherein the data transfers between the first rank and the memory bus through the circuitry are registered data transfers and the circuitry is configured to add a predetermined amount of time delay for each registered data transfer through the circuitry such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.

28. A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

logic coupled to the printed circuit board and configured to receive a set of input control and address signals associated with a read or write memory command via the memory bus and to output a set of registered control and address signals in response to the set of input control and address signals, the set of input control and address signals including a plurality of input chip select signals, the set of registered control and address signals including a plurality of registered chip select signals corresponding to respective ones of the plurality of input chip select signals, the plurality of

registered chip select signals including a registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value;

memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, wherein the plurality of N-bit wide ranks are configured to receive respective ones of the plurality of registered chip select signals, wherein a first N-bit wide rank receiving the registered chip select signal having the active signal value is configured to receive or output a first burst of N-bit wide data signals and a first burst of data strobes associated with the read/write command;

circuitry between data and data strobe signal lines in the memory bus and corresponding data and data strobe pins of the memory devices, wherein the circuitry includes logic pipelines configured to enable data transfers between the first rank and the memory bus in response to the first read or write memory command, wherein respective N-bit wide data signals of the first burst of N-bit wide data signals and respective data strobes of the first burst of data strobes are transferred between the first rank and the memory bus through the circuitry in accordance with an overall CAS latency of the memory module; and

wherein the data transfers between the first rank and the memory bus are registered data transfers; and

wherein the circuitry is configured to add a predetermined amount of time delay for each data transfer between the memory controller and the memory devices such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.

CERTIFICATE OF INTEREST

Undersigned counsel certifies that the following information is accurate and complete to the best of counsel's knowledge:

1. **Represented Entities.** Fed. Cir. R. 47.4(a)(1): "The full name of every entity represented in the case by the counsel filing the certificate."

   Micron Technology, Inc.
   Micron Semiconductor Products, Inc.
   Micron Technology Texas, LLC

2. **Real Party in Interest.** Fed. Cir. R. 47.4(a)(2): "For each entity, the name of every real party in interest, if that entity is not the real party in interest."

   None/Not Applicable

3. **Parent Corporations and Stockholders.** Fed. Cir. R. 47.4(a)(3): "For each entity, that entity's parent corporation(s) and every publicly held corporation that owns ten percent (10%) or more of its stock."

   None/Not Applicable

4. **Legal Representatives.** List all law firms, partners, and associates that (a) appeared for the entities in the originating court or agency or (b) are expected to appear in this court for the entities. Do not include those who have already entered an appearance in this court. Fed. Cir. R. 47.4(a)(4).

   Winston & Strawn

5. **Related Cases.** Provide the case titles and numbers of any case known to be pending in this court or any other court or agency that will directly affect or be directly affected by this court's decision in the pending appeal. Do not include the originating case number(s) for this case. Fed. Cir. R. 47.4(a)(5). *See also* Fed. Cir. R. 47.5(b).

   Netlist, Inc. v. Micron Technology, Inc., Case No. 1:22-cv-00136 (W.D. Tex.)

6. Organizational Victims and Bankruptcy Cases. Provide any information required under Fed. R. App. P. 26.1(b) (organizational victims in criminal cases) and 26.1(c) (bankruptcy case debtors and trustees). Fed. Cir. R. 47.4(a)(6).

None/Not Applicable

/s/ Michael R. Rueckheim
MICHAEL R. RUECKHEIM
Counsel for Appellants

June 26, 2024

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STATEMENT OF RELATED CASES

U.S. Patent No. 10,489,314 (the "'314 patent"), which is the subject of the *inter partes* review ("IPR") proceedings on review in this appeal, was previously asserted in the following litigation: *Netlist, Inc. v. Micron Technology, Inc. et al.*, Case No. 1:22-cv-00136 (W.D. Tex.) (this case has not been resolved). Appellants Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas, LLC ("Micron") challenged claims of the '314 patent that is owned by Appellee/Patent Owner ("Netlist").

PRELIMINARY STATEMENT

This is an appeal from two IPR proceedings in which the Board held that the challenged claims of the '314 patent are not unpatentable under 35 U.S.C. § 103. IP2022-00744 challenged '314 patent independent claim 1 and dependent claims 2–3, 5–6, 8–10 and 12–14. IPR2022-00745 challenged '314 patent independent claim 15 and dependent claims 16–20 and 22–27, and independent claim 28 and dependent claims 29–33. The Board erred in determining that Micron had not demonstrated the challenged claims unpatentable.

First, the Board erred in failing to apply the plain and ordinary meaning when construing independent claim 1 (-744 Proceeding), which recites the term "*specified data rate.*" The claim requires that a computer and a memory module communicate at a *specified data rate*, and a first and second memory rank receives/outputs bursts of data at the *specified data rate*. The Board erred in implicitly limiting the term "specified data rate" to a specific unit of measurement expressed in pieces of data per clock cycle, which as limited was the sole element the Board found lacking in the asserted Halbert prior art reference. No support exists for limiting the claim term to this specific unit of measurement. Under the term's plain meaning, which is broader than the Board's implied construction, Halbert clearly teaches multiple ways to configure a specified data rate, including (i) configuring the system to communicate m-bit-wide data transfers at twice the data rate of the prior art

registered DIMM (dual in-line memory module) and (ii) using "strobe signals to clock data" at a rate of one piece of data per strobe cycle. Under the term's plain meaning, Micron demonstrated obviousness.

Second, the Board erred in applying an overly rigid obviousness test in its analysis of independent claims 15 and 28 (-745 Proceeding). Independent claims 15 and 28 recite "logic" on the memory module that (i) *receives* "input chip select signals" and (ii) *outputs* "registered chip select signals *corresponding to* respective . . . input chip select signals," (iii) where the signals have "active" and "non-active" signal values. The Board determined that Micron's analysis for claim 15.6[1] does not sufficiently explain why a skilled artisan would have combined the teachings of active and non-active chip select signals from Halbert's Figures 2 and 3 with Halbert's Figure 4 embodiment, "accounting for the performance impact of not operating ranks 140 and 142 concurrently." Appx31. The Board erred in at least two ways. It was overly rigid in requiring Micron to explain a separate motivation to combine for claim limitations 15.6 and 28.6, when it was undisputed that Micron provided a motivation to combine the teachings of Halbert's Figures 2 and 3 with Halbert's Figure 4 for earlier claim recitals: limitations 15.4, 15.5, 28.4 and 28.5. And it was overly rigid in requiring Micron to demonstrate how the teachings of

[1] The other challenged independent claim 28 in the -745 proceeding includes a near identical recital.

Halbert's Figures 2 and 3 would operate in a "concurrent" ranks mode when Halbert also discloses a "nonconcurrent" ranks mode. Under the proper, more flexible obviousness test required by *KSR v. Teleflex*, and the proper claim construction, Micron demonstrated obviousness.

Third, the Board erred in failing to apply the plain and ordinary meaning when construing independent claims 15 and 28 (-745 Proceeding). The Board implicitly construed these claims to require sending non-active chip select signals to the ranks when that language is simply not present in the claims. The Board used this improper claim construction to reject Micron's identification of why Halbert's active/non-active chip select signal disclosures would be combined with Halbert's Figure 4 embodiment. Under the claims' plain meaning, Micron demonstrated obviousness.

For all these reasons, Micron respectfully requests that the Court vacate the Board's Decision.

STATEMENT OF JURISDICTION

This is a consolidated appeal under 35 U.S.C. § 141(c) from the Final Written Decisions of the Patent Trial and Appeal Board (the "Board") entered on October 30, 2023, in IPR Proceeding Nos. IPR2022-00744 and IPR2022-00745. In those IPR proceedings Micron challenged claims of the '314 patent assigned to Netlist. Micron

timely filed Notices of Appeal on December 29, 2023. This Court has jurisdiction under 35 U.S.C. §§ 141 and 319 and 28 U.S.C. § 1295(a)(4)(A).

STATEMENT OF THE ISSUES

This appeal presents the following issues:

1. In the -744 Proceeding, did the Board err in construing the term "specified data rate" narrower than its plain and ordinary meaning by limiting it to a specific unit of measurement expressed in pieces of data per clock cycle?

2. In the -744 Proceeding, did the Board err in determining that Halbert did not render obvious the specified data rate limitation under the broader plain and ordinary meaning construction when Halbert discloses multiple ways to configure a specified data rate?

3. In the -745 Proceeding, did the Board err in imposing an inflexible obviousness analysis requiring a separate motivation to combine active/non-active registered chip selects in Halbert's Figure 4 disclosure when it was undisputed that: (1) there was motivation to modify the logic in Halbert's Figure 4 to use registered chip selects generally, and (2) Halbert disclosed registered chip selects having active/non-active signal values?

4. In the -745 Proceeding, did the Board err in imposing an inflexible obviousness analysis requiring Micron to explain how Halbert's active/non-active

chip select teachings would operate with Halbert's concurrent rank mode, when it is undisputed that Halbert also disclosed a non-concurrent rank mode?

5. In the -745 Proceeding, did the Board err in construing the claims to require sending non-active registered chip select signals to the claimed ranks when the challenged claims do not recite that language?

STATEMENT OF THE CASE

I. The '314 Patent is Directed to a Memory Module with Data Buffering, Not Communication at a Specified Data Rate or Use of Active/Non-active Registered Chip Select Signals

The '314 patent's application was filed on December 28, 2017, and claims priority through a long series of applications, the earliest being provisional application No. 60/550,668, filed on March 5, 2004. Appx36-37. The patent is directed to a memory module with data buffering, not a novel communication at a specified data rate or a novel use of active/non-active registered chip select signals.

The "Background of the Invention" describes "memory modules" that include a plurality of "dynamic random access memory (DRAM) devices mounted on a printed circuit board (PCB)." Appx73 (1:42-55). These types of modules "are typically mounted in a memory slot or socket of a computer system." Appx73 (2:46-47). The DRAM devices "are generally arranged as ranks or rows of memory," and the ranks "are selected or activated by address and command signals that are received from the [computer system] processor." Appx73 (2:64-66). The address and

command signals may include "rank-select signals, also called chip select signals." Appx73-74 (2:66-3:1).

Figure 9B, an annotation of which is below, depicts a memory module 210 with a plurality of memory devices 30 that are included in two ranks, 32a and 32b. As the figure shows, a computer system sends the memory module 10 a chip select signal CS_0 and the logic circuit 40 outputs corresponding chip select signals CS_{0A} and CS_{0B}. *See* Appx80 (16:27-32) (circuit 40 "receives a set of input address and command signals" and "generates a set of output address and command signals in response"):

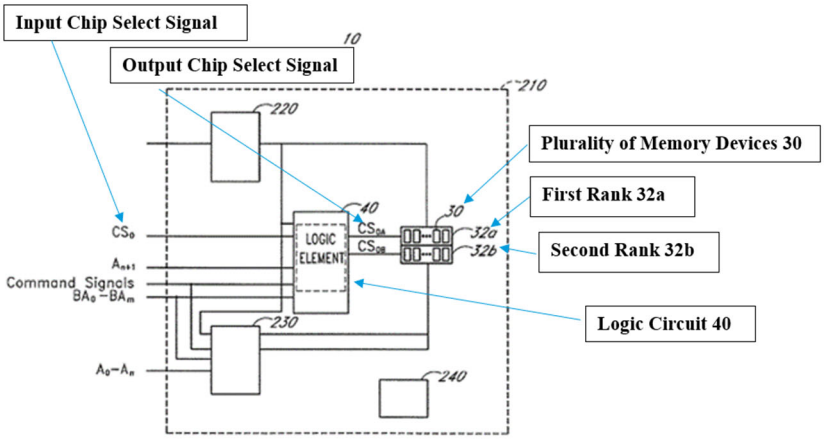


FIG. 9B

Appx61 (Fig. 9B).

The '314 patent does not use the term "specified data rate" outside the claims. Instead, it states that "[m]emory devices 30 compatible with embodiments described herein include" prior art "synchronous DRAM (SDRAM), and double-data-rate DRAM (e.g., SDR, DDR-1, DDR-2, DDR-3)." Appx75 (6:39-43). More

specifically, rather than describe what "specified data rate" means, the patent includes merely generic and minimal disclosure regarding timing and data transfer. For example, it states that "[b]y using synchronous design, such memory modules 400 allow precise control of data transfer between the memory module 400 and the system controller." Appx91 (37:49-52). And it sets forth the following timing diagrams depicting where bursts of data leave a memory device ("DQs") and comparing them to clock (CK), command (Read), and data strobe cycle (DQS) lines:

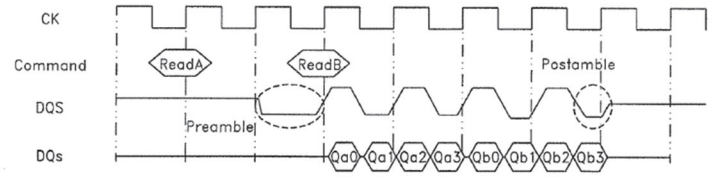


FIG. 6A

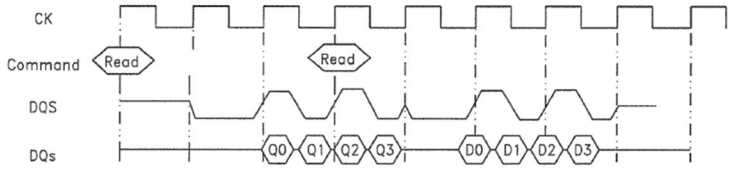


FIG. 6B

Appx56 (Figs. 6A and 6B). The patent also shows the following timing diagram depicting data leaving two memory devices ("data a" and "data b") as compared to clock, command (Read), and data strobe cycle ("strobe a" and "strobe b") lines:

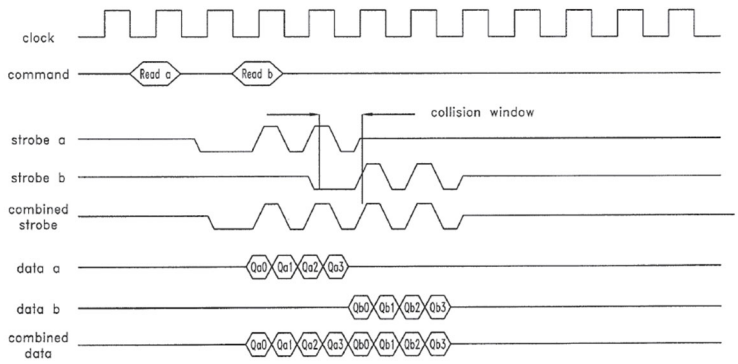


FIG. 7

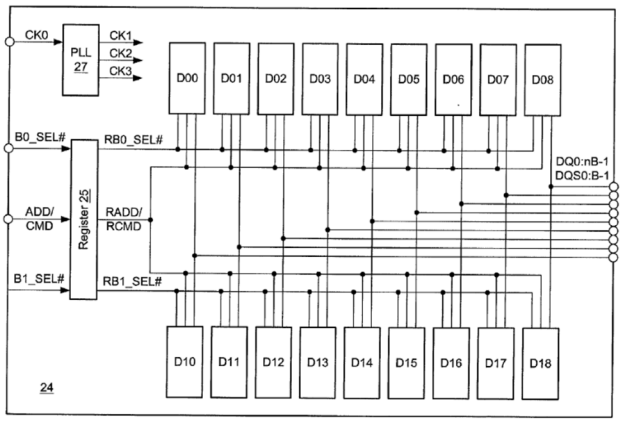
Appx57 (Fig. 7). Lastly, the patent describes that its system is capable of "selecting two ranks concurrently." Appx82 (19:10).

II. The Halbert Reference Teaches Communication at a Specified Data Rate and Active/Non-active Registered Chip Select Signals

The Halbert reference teaches communication at a specified data rate and active/non-active registered chip select signals. Halbert was filed on March 13, 2002, two years before the earliest provisional application identified by the '314 patent. Appx1328.

Halbert's Figure 2, copied below, clearly discloses registered chip select signals. It depicts an exemplary *prior art* module "for a registered DIMM," (Appx1340 (¶13)), "containing eighteen memory devices arranged in two banks, one containing devices D00-D08 and the other containing devices D10-D18":

Fig. 2
(Prior Art)



Appx1339 (¶9), Appx1330 (Fig. 2). It further shows that the module receives input bank select signals B0_SEL# and B1_SEL# and provides corresponding registered output chip select signals RB0_SEL# and RB1_SEL#.[2]

Halbert's Figure 3 builds upon Figure 2 by depicting an exemplary prior art timing diagram "for the Registered DIMM of Fig. 2," which shows chip select signals that can be active or non-active. Appx1340 (¶14). The diagram, copied below, depicts data leaving the two banks (DQ) as compared to clock (CLK), command and address (CMD and ADD), input chip select (B0_SEL#, B1_SEL#), registered command and address (RCMD and RADD), registered chip select (RB0_SEL#, RB1_SEL#), and data strobe cycle (DQS) lines:

[2] It is undisputed that while the use of the terms "ranks" and "banks" may technically have different definitions, practically speaking, they operate the same. Both identify a group of memory devices that are selectable by a chip select. Therefore, these different names are inconsequential for purposes of this appeal. *See* Appx4034.

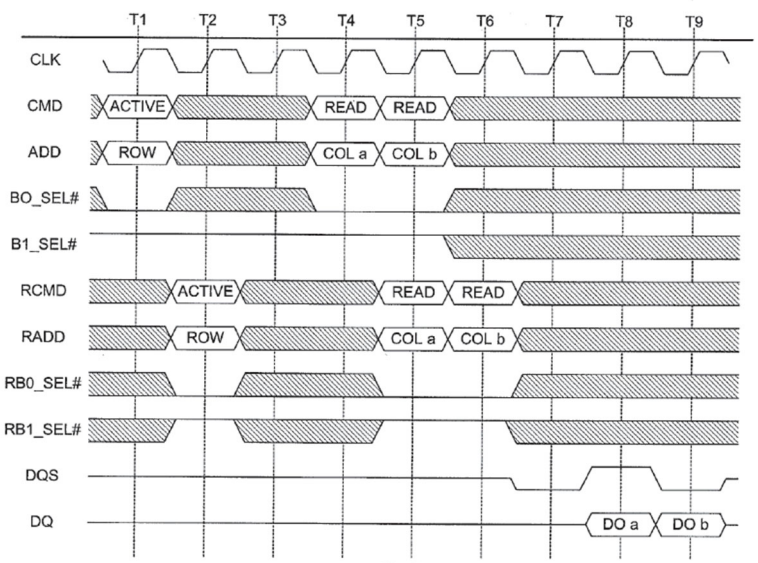


Fig. 3
(Prior Art)

Appx1331 (Fig. 3). And it shows the chip selects in "low" (active) and "high" (non-active) states on the B0_SEL#, B1_SEL#, RB0_SEL#, and RB1_SEL# lines. *See also* Appx1339 (¶10) (discussing "tak[ing] B0_SEL# low to select bank 0").

Halbert's Figure 4 (copied below) depicts "a block diagram for a memory module according to one embodiment of the [Halbert] invention":

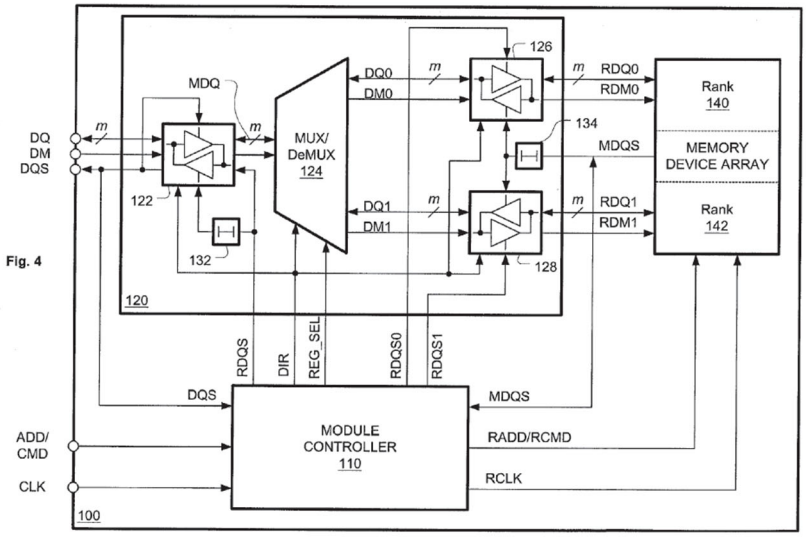


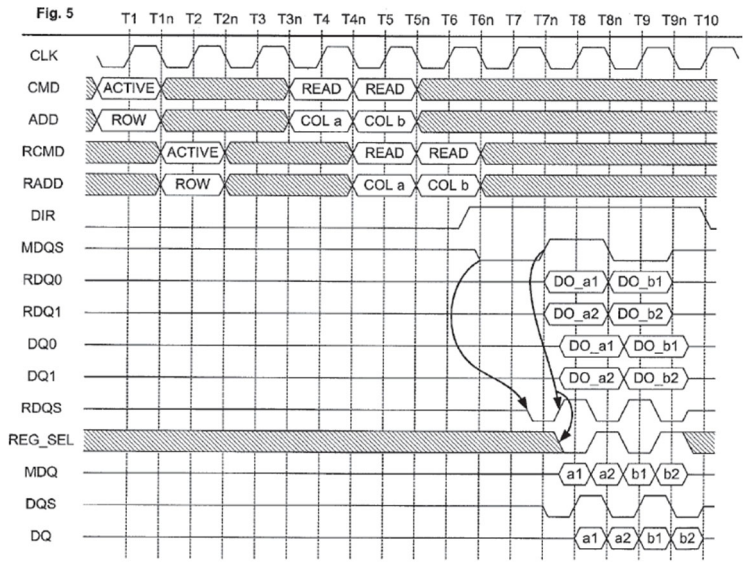
Fig. 4

Appx1332 (Fig. 4); Appx1340 (¶15). It shows a first rank of memory devices 140, a second rank of memory devices 142, and a circuit logic 110 labeled "module controller." And it depicts the logic (module controller 110) receiving and outputting address and command signals but does not explicitly depict chip select signals. Halbert's claim 7, however, recites that "the controller supplies rank selection signals." Appx1344 (Cl. 7).

In explaining the data rate setting, Halbert describes in terms of a "[d]ata interface circuit 120" that "provides for m-bit-wide data transfers between the module and the system memory data bus, and for R×m-bit-wide data transfers between the interface circuit and the memory device array." Appx1341 (¶30). More specifically, in Fig. 4, "R=2, *i.e.*, the memory device array comprises two memory device ranks 140 and 142." Appx1341 (¶30). Notably, as shown in Halbert's Figure 4, each rank (140 and 142) is connected with an "m" bit wide line (RDQ0 and RDQ1), and data exits the module over another "m" bit wide line (DQ).

Like the '314 patent, Halbert also discusses data rates in terms of using "synchronous DRAM (SDRAM) devices including double-data-rate (DDR) SDRAM devices." Appx1343 (¶61). Halbert teaches that it "describes a DIMM that can, with the same type of devices, number of devices, and data signal pins as the dual-bank registered DIMM, provide twice the data rate of the registered DIMM." Appx1340 (¶24).

Halbert's Figure 5 shows examples of specified data rates. It depicts data ("DO_a1," "DO_a2," "DO_b1," and "DO_b2") leaving two ranks (on RDQ0 and RDQ1) and leaving two registers (on DQ0 and DQ1). Figure 5 further depicts corresponding data ("a1," "a2," "b1," and "b2") leaving the module (on DQ). And it compares this data to clock (CLK), command and address (CMD and ADD), registered command and address (RCMD and RADD), direction (DIR), and data strobe cycle (MDQS, RDQS, and DQS) lines:



Appx1333 (Fig. 5). MDQS is the data strobe cycle line synchronized per each piece of data leaving the ranks (on RDQ0 and RDQ1). As the figure illustrates, a data strobe cycle size transition exists from MDQS to RDQS in connection with the REG_SEL signal. *See* Appx1333 (Fig. 5) and Appx1342 (¶48). DQS is the data strobe line synchronized per each piece of data leaving the module (on DQ). Appx1342 (¶40).

Like the ’314 patent, Halbert describes modes where the system is capable of “selecting two ranks concurrently.” Appx1341 (¶30) (“Generally, multiple ranks will receive the same address and commands, and will perform memory operations with the interface circuit concurrently.”). Halbert also discloses a nonconcurrent rank mode. Appx29-31.

III. The -744 IPR Proceeding

A. Micron’s Petition Demonstrated that Halbert Renders Obvious the “Specified Data Rate” Limitations and The Challenged Claims as a Whole

Micron filed its -744 IPR petition on March 30, 2022, demonstrating that Halbert renders obvious the challenged claims and the “specified data rate” limitations. The -744 petition challenged claims 1–2, 6, 8 and 12–14 as obvious in view of Halbert and a skilled artisan’s (“POSITA”) knowledge. Appx235. It also challenged claims 3 and 9–10 as obvious in view of Halbert and a reference named JESD21-C. Appx235. And it challenged claim 5 as obvious in view of Halbert and a reference named JESD79-2A. Appx235. JESD21-C and JESD79-2A are prior art SDRAM specifications published by the industry standards body: JEDEC. Appx245-Appx248.

Micron identified in its petition the level of ordinary skill in the art as a person with various qualifications who would “have been knowledgeable about the design and operation of computer memories, most particularly DRAM and SDRAM

devices that were compliant with various standards of the day, and how they interact with other components of a computer system, such as memory controllers." Appx235. The Board adopted this identification of skill, with the exception of the phrase "at least." Appx6. Micron supported the -744 petition with a detailed expert declaration by Dr. Vojin Oklobdzija. Appx900-Appx1271.

Micron further identified that the Halbert and JESD21-C references were the subject of prior IPRs that found claims in the '314 patent's family unpatentable. Appx238. In addition, Micron explained in the petition that neither party proposed a construction for "specified data rate" in the related litigation. Appx238-239. The -744 petition did not propose any terms for construction. Appx238-239.

Micron focused the petition on Halbert's Figure 4 to show the "components of a memory module" that meet the claim limitations. Appx249-Appx250. Micron explained that the memory module 100, depicted in Halbert's Figure 4, allows for "m-bit wide data transfers" and each of the ranks (140 and 142) similarly allows for "m-bit wide data transfers."[3] In addition, Halbert's embodiment "describes a DIMM that can, with the same type of devices, number of devices, and data signal pins as the dual-bank registered DIMM, provide twice the data rate of the registered

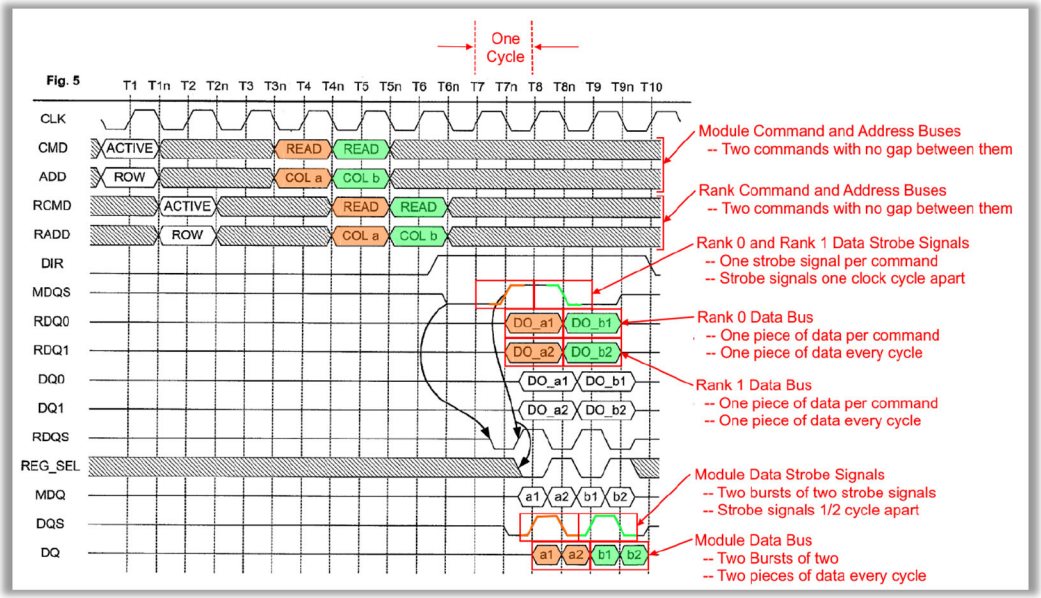
[3] For the ranks, the -744 petition explained that "memory device array" (*i.e.*, ranks 140 and 142 combined) provide for "R×m-bit-wide data transfers" and, in Figure 4, "R=2" because "the memory device array comprises two memory device ranks 140 and 142." Appx250.

DIMM." Appx250. The -744 petition also identified Halbert's timing diagrams and explained that Halbert discloses data strobe cycles "synchronized to its data signals." Appx252.

B. Netlist's -744 Patent Owner Response Urged an Unsupportable Interpretation of "Specified Data Rate"

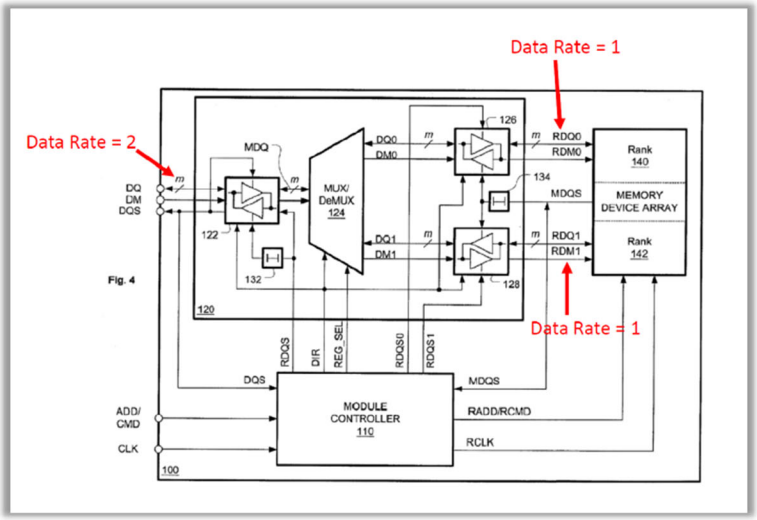
Netlist filed its response on February 7, 2023, after the -744 IPR had instituted, and did not propose claim constructions. Netlist argued, however, that the '314 patent claim 1's use of the term "a specified data rate" in the preamble provides antecedent basis for the use of the term "the specified data rate" in the remainder of the claim and attempted to distinguish Halbert as not disclosing a uniform rate comparing pieces of data to clock signals. Appx1661-1675.

Netlist's Response included the following annotated version of Halbert's Figure 5, arguing that this annotation depicts "***one*** piece of data (DO_a1) is transferred on the RDQ0 bus (shown in Fig. 4 between register 126 and rank 140) in one memory bus clock cycle (from T7n to T8n)" and "***two*** pieces of data (a1 and a2) are transferred on the DQ memory data bus in one clock cycle (from T8 to T9)":



Appx1668.

Netlist also argued the following annotation to Halbert's Figure 4 shows that "Halbert does not teach that data is being transferred through data interface circuit 120 at ***a single, uniform data rate*** as required by the claim." (Appx1669-Appx1671) (emphasis added):



Appx1670. The phrase "a single, uniform data rate" is found nowhere in the claims.

C. Micron's Reply Rebutted Netlist's "Specified Data Rate" Arguments

Micron filed its reply on May 5, 2023, showing that Netlist provided no support for its implicit argument that the term "specified data rate" requires that "the same 'single, uniform data rate' number is used everywhere" the term is recited. Appx1969. Rather, as Micron showed, the '314 patent does not disclose the term "specified data rate" anywhere. Appx1970. Further, "nowhere in the '314 patent is there disclosure associating a single numerical data rate value to both data communicated externally by the memory module and data communicated internally everywhere within the memory module." Appx1970.

Micron also noted that even "Patent Owner's expert concedes, a POSITA would have understood 'a specified data rate' to mean merely that the data rate ***is specified in some way***." Appx1971. Further, Micron identified Halbert's disclosure of a specified data rate in terms of m-bit-wide data transfers "twice the data rate of the registered DIMM." Appx250-51. Micron also explained that Figure 5 depicts that "DQ0 data associated with memory device array rank 140 . . . is at the 'specified data rate' because it has the same clock rate as the DQS [strobe] clock rate that clocks the DQ data out of the memory module to the memory controller." Appx1972-Appx1973. Micron also described Halbert's disclosure associated with a specified rate and noted Netlist's concession on that point:

> Petitioners have shown in Halbert's Fig. 5 that both DO_a1 and DO_b1 are output from the first rank 140 onto bus RDQ0 (Pet., 42), and "DO_a1 is output on the rising edge of the respective set of data strobes of the first burst of data strobes, i.e., MDQS, at T7n, and DO_b1 is output on the falling edge of MDQS at T8n" (*id.*, 43). Thus, the memory devices associated with the first rank 140 in Halbert are configured to receive or output a set of bits on the rising edge of data strobe MDQS, e.g., DO_a1, and a set of bits on the falling edge of data strobe MDQS, e.g., DO_b1. Patent Owner concedes as much, stating that "it is true that DO_a1 and DO_b1 are output on the rising and falling edges of data strobe signal MDQS."

Appx1984.

D. The Board Erred as a Matter of Law in Adopting a Construction for the Phrase "Specified Data Rate" that is Not Consistent with its Plain and Ordinary Meaning

The Board issued the Final Written Decision on October 30, 2024, construing "specified data rate" as follows:

> We determine that the plain language of claim 1 requires that later recitations of "the specified data rate" refer to the same data rate as "a specified data rate" in the preamble, which is the rate at which data are communicated between the memory module and the memory controller.

Appx8.

The Board did not address Micron's position that Halbert teaches a "specified data rate" of m-bit-wide data transfers at "twice the rate of the registered DIMM." Instead, the Board distinguished Halbert as disclosing a rate of *one piece of data per clock cycle* for communications with the *ranks*, and *two pieces of data per clock cycle* for communication with the *module*, stating:

> As shown in Halbert's Figure 5, over one clock cycle (T7n–T8n), each of ranks 140 and 142 outputs one piece of m-bit-wide data, and over one clock cycle (T8–T9), those two pieces of m-bit-wide data are output on line DQ to the system memory data bus.

Appx12.

The Board also did not address Micron's position that Halbert also teaches a specified rate of one piece of data synchronized per strobe clock cycle. Instead, the -744 Decision discussed the REG_SEL signal in terms of controlling "the MUX/DeMUX 24 . . . thereby allowing the memory module to operate at twice the rate of each of the ranks." Appx13.

IV. The -745 IPR Proceeding

A. Micron Demonstrated that Halbert Renders Obvious Limitations [15.6] and [28.6] and the Challenged Claims as a Whole

Micron filed its -745 IPR petition on March 30, 2022, challenging claims 15–20 and 22–33 as obvious in view of Halbert and JESD21-C. Appx2368. JESD21-C is a prior-art SDRAM specification published by the industry standards body: JEDEC. Appx2378-Appx2379.

Micron identified the level of ordinary skill in the art as a person with various qualifications who would "have been knowledgeable about the design and operation of computer memories, most particularly DRAM and SDRAM devices that were compliant with various standards of the day, and how they interact with other components of a computer system, such as memory controllers." Appx2368. The

Board adopted that identification of skill, with the exception of the phrases "at least." Appx21. Micron supported the -745 petition with a detailed expert declaration by Dr. Vojin Oklobdzija. Appx3041-Appx3412.

Micron noted that the Halbert and JESD21-C references were the subjects of other IPRs that found claims in the '314 patent's family unpatentable. Appx2371. Micron also noted the parties' respective proposed construction from the related litigation, in which neither party proposed a construction for limitations [15.6] and [28.6]. Appx2371-72. The -745 petition did not propose any terms for construction. Appx2371-72.

Micron's petition focused mostly on Halbert's Fig. 4 and its associated disclosure to show the "components of a memory module" that meet the claim's apparatus limitations. Appx2380-Appx2381. Micron also established that Halbert's Fig. 2 disclosure shows registered chip select signals. Appx2392-Appx2396. More specifically, Halbert discloses limitation [15.5], Appx2392-Appx2396, which recites "the first set of registered address and control signals including a first plurality of registered chip select signals corresponding to respective ones of the first plurality of input chip select signals." Appx94 (44:63-66). Netlist did not dispute this fact. Appx3728.

Micron further demonstrated that Halbert's explanation of Halbert's Fig. 2 shows that the registered chip select signals identified for limitation [15.5] would

include a first registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value, as recited in limitation [15.6]. Appx2385-2397.

Micron explained why a POSITA would have been motivated to combine the teachings associated with Halbert's Fig. 2 with the teachings associated with Halbert's Fig. 4, *i.e.*, why a POSITA would have included registered chip select signals in Fig. 4, as part of the discussion of limitations [15.4] and [15.5]. Appx2385-Appx2396. The petition also identified that limitation [15.6] refers back to the teachings regarding the first plurality of registered chip select signals of limitation [15.5]. Appx2396. The -745 petition showed that the teachings of Halbert's Fig. 2 and Fig. 4 are directed to the design of the same type of memory module architecture—registered DIMMs. Appx2386; Appx2393. The -745 petition further identified that module controller 110 in Fig. 4 would have a plurality of chip selects as inputs because there are multiple memory device ranks 140 and 142, and chip selects would select whether data is transferred to/from memory device rank 140 or 142. Appx2425.

B. Netlist Did Not Dispute the Motivation to Combine the Selected Signals Teaching from Halbert's Fig. 2 with Halbert's Fig. 4 Embodiment

Netlist filed its response on February 7, 2023, after the -745 IPR instituted in which it did not dispute the critical teachings of Halbert. The response raised

multiple grounds of purported differences but did not propose claim constructions other than plain meaning. Although Netlist generally argued that limitation [15.6] is not obvious Appx3728-Appx3738, *Netlist did not dispute that Halbert's Fig. 2 discloses registered chip select signals*. Specifically, Netlist did not dispute that Halbert renders obvious limitation [15.5], which recites "the first set of registered address and control signals including a first plurality of registered chip select signals corresponding to respective ones of the first plurality of input chip select signals." Appx94 (44:63-66).

C. Micron Rebutted Netlist's Arguments and Demonstrated Undisputed Facts Dictating that the Challenged Claims are Rendered Obvious

Micron replied on May 5, 2023. Micron identified that the petition "articulated why a POSITA would have been motivated to combine the teachings of Halbert's Fig. 2 and JESD21-C with Halbert's Fig. 4 during its discussion of the related [earlier] limitations [15.4 and 15.5] [that] introduce[ed] a first plurality of input chip select signals (Pet., 20-27) and a first plurality of registered chip select signals (id., 27-31), which Limitation [15.6] refers back to the first plurality of registered chip select signals." Appx4031. Micron further identified that based on the reasoning provided in the petition for "why a POSITA would have been motivated to combine the teachings of Halbert's Fig. 2 and JESD21-C with Halbert's Fig. 4 for earlier Limitations [15.4]-[15.5], it naturally follows that a POSITA would continue to

apply further teachings of the secondary references to subsequent recitations to the same elements (*i.e.*, the first plurality of registered chip select signals)." Appx4031-Appx4032. Micron noted that the reasoning provided in the "Petition for Limitation [15.5] [explained] why a POSITA would have included registered chip select signals in Fig. 4." Appx4032.

Micron further noted that limitation [15.6] directly relates to how the registered chip select signals identified for limitation [15.5] normally function, *i.e.*, limitation [15.6] is directed to using the registered chip select signals in the manner they normally operate, as illustrated in Halbert's Fig. 3. Appx4032-Appx4033 As Micron explained, the detailed obviousness analysis for limitation [15.5] regarding the combined Halbert Fig. 2 and Fig. 4 teachings also covered limitation [15.6] because the obviousness analysis for limitation [15.5] resulted in the teachings of Halbert's Fig. 2 registered chip select signals being incorporated into Fig. 4, and limitation [15.6] is directed to using those same registered chip select signals of limitation [15.5] in the manner they normally operate. Appx4033.

Micron summarized the undisputed obviousness posture of limitation [15.6] after the petition and Netlist's response to highlight how the prior art combination rendered the claims obvious:

> Patent Owner does not rebut that Ground 1 renders obvious the use of registered chip select signals in Fig. 4 (Limitation [15.5]). And prior art Fig. 3 shows that use of active and non-active registered chip select signals was

> well-known in the art. Thus, it would have been obvious to apply Fig. 3's disclosure of the use of active and non-active registered chip select signals to the unrebutted registered chip select signals shown to be obvious to include in Fig. 4.

Appx4033-Appx4034.

D. The Board Erred in its Final Written Decision by Incorrectly Analyzing Obviousness Inflexibly and Incorrectly Construing Limitations [15.6] and [28.6] to Find the Challenged Claims Not Unpatentable

The Board issued its Final Written Decision on October 30, 2023, stating that it "need not construe expressly any claim terms to decide the issues before us." Appx21. But the decision did just that. Specifically, the decision implicitly construed claim limitations [15.6] and [28.6] as limitations that require that both the "active and non-active chip select signals" be applied (or sent) to the memory devices (ranks 140 and 142). Appx30-Appx33 (stating "Petitioner has not provided adequate reasoning to apply active and non-active chip select signals to ranks 140 and 142, as discussed above").

The Board acknowledged that Micron provided reasoning for why a POSITA would have been motivated to combine the teachings associated with Halbert's Fig. 2 with the teachings associated with Halbert's Fig. 4, *i.e.*, why a POSITA would have included registered chip select signals in Fig. 4, as needed to support the obviousness showing for limitations [15.4] and [15.5] that limitation [15.6] refers back to, stating: "Petitioner presents reasoning as to why a person of ordinary skill in the art would

have included chip select signals in Halbert's Figure 4 device. *See* Pet. 20-31 (addressing limitations 15.4 and 15.5)." Appx27. Because limitation [15.5] expressly recites "the first set of registered address and control signals including a first plurality of registered chip select signals corresponding to respective ones of the first plurality of input chip select signals," (Appx94 (44:63-66)), the Board acknowledged that Halbert's Fig. 2 disclosed registered chip select signals and that it was obvious for those registered chip select signals shown in Halbert's Fig. 2 to be used in Halbert's Fig. 4. Appx27.

With respect to whether Halbert's Fig. 2 discloses that the registered chip select signals identified for limitation [15.5] would include chip select signals with active/non-active signal values, the Board answered that question affirmatively, stating: "Petitioner's contentions correctly assert that Halbert's Figure 2 memory device would have active and non-active signals . . . ." Appx29-Appx30.

Despite the foregoing facts establishing obviousness, the Board found the challenged claims nonobvious based on a requirement that Micron provide motivation to include registered chip select signals having active/non-active signal values in Halbert's Figure 4 disclosure, stating: "Petitioner's contentions that using chip select signals would have been obvious in Halbert's Figure 4 do not sufficiently address the particular requirement of having a 'first plurality of registered chip selects signals including . . . an active signal value and . . . a non-active signal

value.'" Appx31. The Board erred for the reasons Micron sets forth in further detail below.

SUMMARY OF THE ARGUMENT

This Court should vacate the Board's decision and remand.

-744 Proceeding:

I. The Board erred in implicitly construing the term "specified data rate" inconsistent with its plain and ordinary meaning by improperly limiting that term narrowly to a specific unit of measurement comparing pieces of data to clock signals. The plain and ordinary meaning of the term "specified data rate" is not so limited. It is a broad term that generally encompasses specifying, *i.e.*, constraining, a data rate in some manner. No support exists for limiting this term to only a rate comparing pieces of data to clock signals.

II. Halbert discloses the claimed "specified data rate" feature in at least two ways. First, Halbert discloses specifying a data rate of m-bit-wide data transfers at twice the data rate of the prior art registered DIMM. This rate is properly defined by a relationship of (i) the data outputted from the module *compared to* (ii) the data outputted from either rank—a relationship that is not precluded by the broad term "rate." Second, Halbert discloses a specified data rate of one piece of data synchronized per strobe cycle.

-745 Proceeding:

I. The Board erred in determining that the challenged claims were nonobvious because that determination was based on the Board's misapplication of the law of obviousness as set out by the Supreme Court in *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398 (2007). Specifically, the Board applied an inflexible obviousness analysis that precluded recourse to a common sense obviousness determination in requiring a separate motivation to include select signals having active/non-active signal values in Halbert's Figure 4 disclosure. The Board's overly rigid obviousness analysis ignored that it was undisputed that: (i) Halbert renders obvious the use of chip select signals; (ii) Halbert described the prior art's use of active/non-active select signals; and (iii) active/non-active states are how select signals normally function. Common sense dictates that these facts, as supported by Micron's apparatus-focused obviousness rationale, are sufficient to render limitations [15.6] and [28.6] and, as a result, the challenged claims obvious. The Board's determination that limitations [15.6] and [28.6] nonetheless render the challenged claims nonobvious was therefore contrary to *KSR* and this Court's precedent, and erroneous as a matter of law.

II. The Board's determination that the challenged claims were nonobvious was also erroneous as a matter of law, as contrary to *KSR*, for rigidly requiring an explanation as to how Halbert's teaching of active/non-active select signals would

operate with Halbert's concurrent rank mode, when it was undisputed that Halbert also discloses a non-concurrent rank mode. *KSR* requires a more flexible analysis. This Court also has held that obviousness does not require a showing that the combination meets the claims "in all modes of operation." *See ParkerVision, Inc. v. Qualcomm Inc.*, 903 F.3d 1354, 1361 (Fed. Cir. 2018).

III. The Board's claim construction of claims 15 and 28 is erroneous as a matter of law because the construction improperly requires that both the "active and non-active chip select signals" be applied (or sent) to the memory devices (ranks 140 and 142). These claims make no reference whatsoever to non-active select signals being sent to the memory devices or ranks. The Board erred in construing these limitations to require more than what is expressly claimed.

STANDARD OF REVIEW

This Court reviews *de novo* "the Board's ultimate claim constructions and any supporting determinations based on intrinsic evidence." *Personalized Media Commcn's LLC v. Apple Inc.*, 952 F.3d 1336, 1339 (Fed. Cir. 2020). This Court reviews the Board's ultimate obviousness determination *de novo* and underlying factual findings for substantial evidence. *See Ariosa Diagnostics v. Verinata Health, Inc.*, 805 F.3d 1359, 1364 (Fed. Cir. 2015).

ARGUMENT

I. -744 IPR Proceeding: The Board Erred Construing "Specified Data Rate" and Determining this Limitation Missing in the Halbert Prior Art

The Board erred as a matter of law in the -744 Decision by construing the "specified data rate" limitation and finding this limitation missing from the Halbert reference. The Board reviews errors in claim construction *de novo.* *See Personalized Media*, 952 F.3d at 1339.

Independent claim 1 recites, *inter alia*:

> A memory module operable in a computer system to communicate data with a memory controller of the computer system ***at a specified data rate*** via a N-bit wide data bus
>
> . . .
>
> a first rank configured to receive or output the first burst of N-bit wide data signals and the first burst of data strobes at ***the specified data rate*** in response to the first memory command, and a second rank configured to receive or output the second burst of N-bit wide data signals and the second burst of data strobes at ***the specified data rate*** in response to the second memory command.

Appx93 (42:12-14, 42:31-38). The parties did not dispute that this claim should be construed according to its plain and ordinary meaning. The Board, however, erred in its decision by implicitly construing this term to be limited to a specific unit of measurement—a piece of data per clock cycle—and thereby departing from its plain and ordinary meaning. No support exists for this narrow interpretation. Under the

proper and broader plain meaning, Halbert teaches a specified data rate, and the Court should vacate the Board's decision.

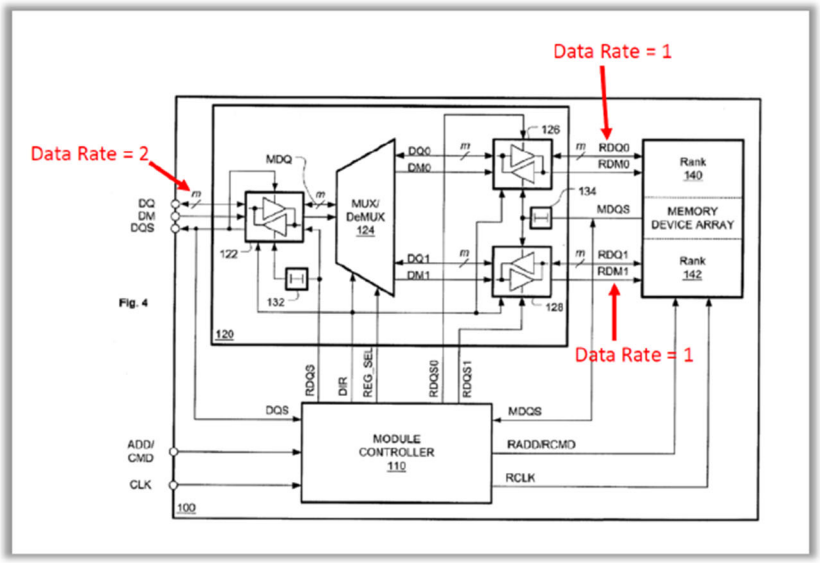
A. The Board Erred in Construing "Specified Data Rate"

Claims are construed according to their plain and ordinary meaning absent lexicography or clear disavowal. *Golden Bridge Tech., Inc. v. Apple Inc.*, 758 F.3d 1362, 1365 (Fed. Cir. 2014). Here, "specified data rate" should be afforded its plain meaning because there is no lexicography or disavowal. Indeed, the '314 patent ***does not use the term*** "specified data rate" ***at all*** within the specification. Moreover, neither party disputed that the term should be given its plain and ordinary meaning.

The Board erred in implicitly construing the term "specified data rate" as narrowly limited to only a measurement unit comparing pieces of data to clock signals, contrary to its plain meaning. As a preliminary issue, the Board initially stated its construction of this term correctly and more broadly as "the rate at which data are communicated between the memory module and the memory controller." Appx8. The Board, however, ultimately ***applied*** a narrower construction in its holding by distinguishing Halbert's ranks as each outputting "one piece of m-bit-wide data" over one clock cycle and Halbert's module as outputting "two pieces of m-bit-wide data" per one clock cycle. Appx12. This holding evidences an implicit claim construction that is unsupportable. *See Google LLC v. EcoFactor, Inc.*, 92

F.4th 1049, 1056 (Fed. 2024) (finding "implicit claim constructions even when the Board does not recognize that it is construing a claim").

The Board's narrow interpretation resulted from Netlist's attempt to distinguish the Halbert prior art. Specifically, Netlist argued that Halbert's Figure 5 demonstrates that "one ***piece of data*** (DO_a1) is transferred on the RDQ0 bus . . . ***in one*** memory bus ***clock cycle*** . . . [and] ***two*** pieces of data (a1 and a2) are transferred on the DQ memory data bus ***in one clock cycle***." Appx1669 (modified emphasis from original). Netlist provided the following annotation of Halbert's Figure 4 to demonstrate its pieces-of-data-per-clock interpretation of the data rate:



Appx1670 (Fig. 4 (annotated)).

The Board, in fact, recognized during oral argument that Netlist ultimately was making a claim construction argument for this term:

> JUDGE GALLIGAN: Okay. And because I'm looking at the petitioners' reply it in 744 case, the first page of it. And it says, patent owner construes the specified data rate limitations to mean that the same ***single uniform data rate number*** is used everywhere to specify data rates recited. You know, it sounds like you, you are on notice of ***their understanding of the claim***. Is that is not the case?
>
> MR. RUECKHEIM: We did, we did see how they were trying to construe the claim. And that's how we responded to it . . . and I think this is also highlighted by opposing counsel's argument, just now.

Appx4371 (84:7-16) (emphasis added).

Limiting the claim term to a specific "pieces of data per clock" measurement unit is unsupported. No evidence—intrinsic or extrinsic—requires limiting "specified data rate" to these units. *See Thorner v. Sony Comput. Ent. Am. LLC*, 669 F.3d 1362, 1367 (Fed. Cir. 2012) (a patentee "is free to choose a broad term and expect to obtain the full scope of its plain and ordinary meaning unless the patentee explicitly redefines the term or disavows its scope"). Nor does expert analysis identify any lexicography or clear disclaimer that would suggest a POSITA would have understood the term as limited to these units. To the contrary, Netlist's expert admitted that the term "specified data rate" does not have a special industry meaning, and the plain language broadly refers to a data rate that is only specified or constrained in some way:

> Q. You're not opining that the term specified data rate has some type of special meaning in this field, correct?
>
> . . .

> A. I have interpreted that phrase as a POSITA would at that time and in the context of the '314 patent to be a data rate that is specified in some way.
>
> . . .
>
> Q. What does the word specified mean to you?
>
> A. Constrained in some way.

Appx2129 (39:15-22), Appx2130 (42:16-18).

The record demonstrates that the meaning of "specified data rate" is broad and can be expressed in a number of different ways. For example, the '314 patent and the Halbert prior art reference both discuss data rates in terms of m-bit (or N-bit) wide data transfers. Appx93 (42:17-23); Appx1341 (¶30). Both references also discuss data rates in terms of using prior art standardized SDRAM DDR (double data rate) memory devices. Appx75 (6:39-43), Appx91 (37:36-44); Appx1343 (¶61).

Both references further demonstrate that the meaning of "specified data rate" is broader than that adopted by the Board by discussing rates in terms of data transfers synchronized per strobe signal. Appx91 (37:52-53) ("Data transfer can take place on both edges of the DQS signal."); Appx1333 (Fig. 5), Appx1343 (¶58) ("[T]he illustrated examples use source-synchronous strobe signals to clock data, common-clock signaling can also be used[.]"). Netlist's expert also admitted during deposition that data rates can be characterized in terms of pieces of data per strobe cycle:

> Q. Okay. With respect to Figure 1, if the first rank outputs a respective set of bits on both edges of each of the respective set of data strobes, what is a data rate of that first rank?
>
> . . .
>
> A. One way to describe that ***data rate*** would be to say that it -- the data was being transferred at one datum per phase.

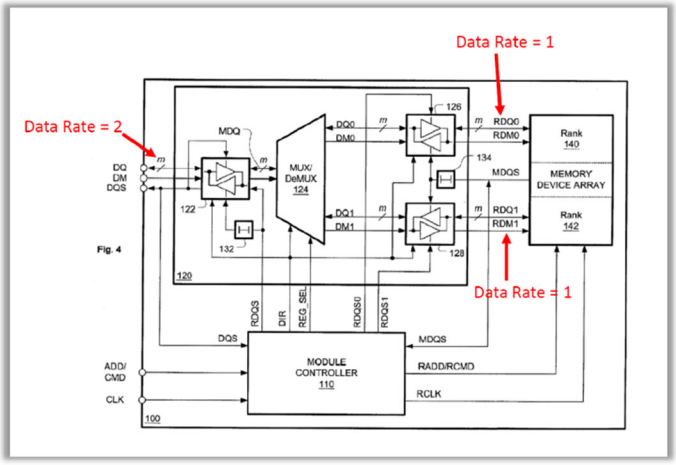
Appx2131 (48:8-17) (emphasis added).

In sum, the Board erred as a matter of law in implicitly construing the claim more narrowly than its plain and ordinary meaning.

B. Halbert Teaches a "Specified Data Rate"

Under the plain meaning construction, Halbert clearly teaches a system with the claimed "specified data rate." For example, Halbert teaches that it specifies a data rate for m-bit-wide communications at twice the data rate of the prior art registered DIMM. Appx1340 (¶24). Halbert does not discuss a system with an unspecified random data rate that will change over time. Nor does Halbert discuss a system configured to have an unspecified data rate that depends upon outside signaling to set the data rate on a command-by-command basis. Indeed, Halbert's Figures 5 and 6 depict timing diagrams that specify the data rates for two consecutive operations and depict *repeatable* timings that do not *vary* even for consecutive commands**.**

Netlist's annotation of Halbert's Figure 4 (below for reference) further demonstrates Halbert's teaching of a specified data rate of m-bit-wide communications at twice the data rate of the registered DIMM. More specifically, in the annotated figure below, memory module 100 communicates data with a memory controller of a computer system at a specified data rate of two pieces of DQ data (left side of figure) per one piece of the RDQ0 or RDQ1 data being communicated to and from the ranks (right side of figure):

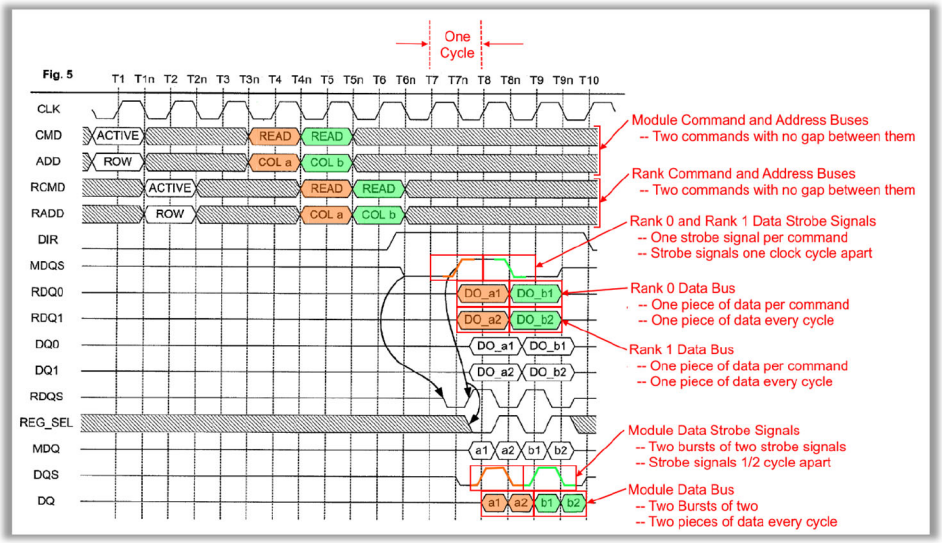


Appx1670 (Fig. 4 (annotated)). Configuring a system to communicate (two DQs) per (one RDQ0 or one RDQ1) is an actual setting for the memory module, a setting that specifies a constrained data rate.

Further, the claims require nothing more than the specified data rate shown in Netlist's annotated Figure 4 above. The claims' recital of a "memory module . . . to communicate data with . . . the computer system at a specified data rate" is met by Halbert's disclosed rate of (two DQs) per (one RDQ0 or one RDQ1). The claims'

recital of "rank[s] configured to receive or output the first burst of N-bit wide data signals and the first burst of data strobes at the specified data rate" is met by Halbert's disclosed rate of (one RDQ0 or one RDQ1) per (two DQs). And it makes no difference if one labels Halbert's rate as (i) (two DQs) per (one RDQ0 or one RDQ1) or (ii) (one RDQ0 or one RDQ1) per (two DQs)—it is the same data rate.

Halbert also teaches a specified data rate in terms of pieces of data per strobe cycle. For example, Halbert teaches that its "illustrated examples use source-synchronous ***strobe signals to clock data***, [but] common-clock signaling can also be used." Appx1343 (¶58). In addition, Halbert teaches, with regard to Halbert's Figures 4 and 5, that it uses strobes synchronized to the data signals. *See* Appx1341 (¶38) ("MDQS will comprise multiple strobes, each device in device array 140/142 supplying at least one strobe synchronized to its data signals."). Halbert's Figure 5 (*see* Netlist's annotated version copied below) depicts these strobe cycles on the MDQS, RDQS, and DQS lines:



Appx1668 (Fig. 5 (annotated)).

It also specifies a data rate of one "piece of data" per strobe cycle throughout the entire system. For example, at the MDQS/RDQ0 level (corresponding to rank communications) there is one "DO_a1" per rising strobe edge of MDQS and one "DO_a2" per falling strobe edge of MDQS. Then, "REG_SEL . . . determines whether DQ0 or DQ1 will be supplied to buffer" (*see* Appx245) and a strobe clock cycle shift (*see* the arrows connecting MDQS and RDQS/REG_SEL in Figure 5) results in a shorter strobe cycle. This strobe shift results in the same specified data rate at the DQ/DQS level (corresponding to module communications): one "a1" per rising edge of DQS strobe and one a2 data per falling edge of DQS strobe. Thus, the same specified data rate exists for the module and rank communications.

In comparison, the Board's Decision focused on a very narrow view of the term "specified data rate," ignoring that Halbert specifies a data rate in a number of

ways, including (i) an m-bit-wide data rate of two pieces of DQ data per one piece of RDQ0 (or RDQ1) data per rank and (ii) one piece of data per strobe cycle throughout the system. The Board thus erred in failing to recognize and address these specified rates, and therefore, this Court should vacate the Board's Decision.

II. -745 IPR Proceeding: The Board Erred Applying an Inflexible Obviousness Test[4]

The Board erred by applying an overly rigid obviousness analysis that required a more exacting explanation of the motivation to combine than *KSR* mandates. *See KSR*, 550 U.S. at 415 (rejecting "rigid approach" because "[t]hroughout this Court's engagement with the question of obviousness, our cases have set forth an expansive and flexible approach"). The Court reviews this issue *de novo*. *See Ariosa Diagnostics*, 805 F.3d at 1364.

More specifically, the Board erred in making the following determination:

> Petitioner's analysis for limitation 15.6 does not sufficiently address Halbert's Figure 4, much less "explain why a person of ordinary skill in the art would have combined elements from specific references in the way the claimed invention does," accounting for the performance impact of not operating ranks 140 and 142 concurrently.

Appx31. This determination was legal error for at least two primary reasons. First, the Board was overly rigid in requiring Micron to explain a separate motivation to

[4] While the argument in this section focuses primarily on limitation 15.6, the argument applies equally to limitation 28.6.

combine with respect to the chip select recitals in claim limitations 15.6 and 28.6, when Micron's motivation to combine for the chip select recitals in claim limitations 15.4, 15.5, 28.4, and 28.5 were undisputed. Second, the Board was overly rigid in requiring Micron to demonstrate how non-active signals would operate in Halbert's "concurrent ranks" mode, when Halbert also disclosed a "nonconcurrent ranks" mode.

A. *KSR* Requires a Flexible Approach to Obviousness Analysis

In *KSR*, the Supreme Court emphasized that the obviousness inquiry requires flexibility and "observed that common sense can be a source of reasons to combine or modify prior art references to achieve the patented invention." *Plantronics, Inc. v. Aliph, Inc.*, 724 F.3d 1343, 1354 (Fed. Cir. 2013) (citing *KSR*, 550 U.S. at 420). This Court has noted that, under *KSR*,

> motivation to combine may be found explicitly or implicitly in market forces; design incentives; the interrelated teachings of multiple patents; any need or problem known in the field of endeavor at the time of invention and addressed by the patent; and the background knowledge, creativity, and common sense of the person of ordinary skill.

Id. (internal quotations omitted).

Acknowledging that "there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness" (*KSR*, 550 U.S. at 418 (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006))), the Supreme

Court nonetheless stated: "[H]owever, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *Id.*

Since *KSR*, this Court has elaborated on what is sufficient to support a legal conclusion of obviousness under *KSR*'s flexible approach. In *Wyers v. Master Lock Co.*, 616 F.3d 1231, 1238 (Fed. Cir. 2010), this Court held that a motivation to combine and a reasonable expectation of success exist when "it is simply a matter of common sense" to combine known elements of the prior art to solve a known problem. Then, in *Slot Speaker Techs., Inc. v. Apple Inc.*, 2015-2038, 680 F. App'x 932, 943 (Fed. Cir. Feb. 17, 2017), this Court stated that "[t]here need not be an explicit teaching to combine references in the prior art. Depending on the nature of the technology and the knowledge of those skilled in the art, a motivation to make a particular modification may be a matter of common sense."

B. The Board Erred in Inflexibly Requiring Micron to Demonstrate a Separate Motivation to Combine for Claim Limitations 15.6 and 28.6 when it was Undisputed Motivation to Combine the Same Teachings for Prior Claim Limitations 15.4, 15.5, 28.4, and 28.5 Existed

Under *KSR*'s flexible approach to obviousness, the Board erred in requiring Micron to demonstrate a separate motivation to combine for claim limitations 15.6 and 28.6. Micron demonstrated the undisputed fact that there is a motivation to

combine the same teachings from Halbert's Figures 2 and 3 with Halbert's Figure 4 embodiment with respect to earlier claim limitations.

More specifically, the '314 patent recites "logic . . . configured to receive a first set of input address and control signals" including a "plurality of input chip select signals," (claim limitation 15.4), and the logic is further configured "to output a first set of registered address and control signals" including a "plurality of registered chip select signals," (claim limitation 15.5), wherein the chip select signals have active/non-active signal values (claim limitation 15.6). Appx22.

Micron demonstrated Halbert's Figures 2 and 3 teachings of using bank select signals (B0_SEL# and B1_SEL#). Appx2385-86, Appx2392-94, Appx2396-97. Micron also demonstrated that these signals possess active and non-active states. Appx2396-97. This is how select signals normally operate. Appx4032-33. The active state is used when selecting; the non-active state is used when not selecting. Appx2396-97. The Board agreed with Micron's showing. Appx29-30 ("Petitioner's contentions correctly assert that Halbert's Figure 2 memory device would have active and non-active signals[.]"). Netlist did not and could not dispute Micron's showing. Appx4033-34.

Micron further demonstrated that it would be obvious to modify the logic in Halbert's Figure 4 with the explicit teachings of Figure 2 and Figure 3 to result in the claimed logic that receives and outputs chip select signals as claimed. *See*

Appx27 at 12 ("As outlined above, Petitioner presents reasoning as to why a person of ordinary skill in the art would have included chip select signals in Halbert's Figure 4 device."). The Board agreed with Micron's showing. Appx23-25. Netlist did not and could not dispute Micron's showing. Appx4031-32.

The Board's determination that something more is required to render claim limitation 15.6 obvious fails the flexible approach required by *KSR*. Common sense dictates that Halbert's logic modified to use registered chip select signals as claimed in limitations 15.4 and 15.5 would use registered chip select signals according to the normal (and finite) active/non-active states they possess. Indeed, Halbert explicitly depicts that chip select signals possess active and inactive signal values. Appx2396-97.

Here, as in *KSR*, a known problem exists that chip select signals must possess a state to operate; there are a finite number of known options, *i.e.*, active/non-active states; and modifying Halbert's logic to receive and output both types of chip select signals is not the product of "innovation but of ordinary skill and common sense." *KSR*, 550 U.S. at 421. Indeed, the obviousness showing here is particularly strong, as the teachings are all in one reference, and Halbert's figures are all directed to the same problem: the design of the same type of registered DIMM memory module architecture. Appx2385-86.

Additionally, as in *KSR*, what "matters is the objective reach of the claim" and that the Board's requirement of a "particular motivation" for limitation 15.6 was inflexible. *KSR*, 550 U.S. at 419-20. The claim scope here encompasses logic that receives and outputs chip select signals that operate according to their normal active/non-active states. Halbert teaches use of active/non-active registered chip select signals in Figures 2 and 3, and the Board found it obvious to modify the logic in Halbert's Figure 4 to likewise use those registered chip select signals. Appx23-25. Indeed, Halbert even claims using "rank selection signals." Appx4036. Halbert's teaching of registered chip select signals that have active/non-active signal values is thus well within the objective reach of the challenged claims.

The Board's requirement that, despite this undisputed evidence, Micron provide a separate explanation of the motivation to combine for claim limitation 15.6 is clear error. In light of the undisputed identification of why a POSITA would have been motivated to combine the teachings associated with Halbert's Fig. 2 with the teachings associated with Halbert's Fig. 4 for the earlier limitations [15.4] and [15.5], it naturally follows that a POSITA would continue to apply those ***same teachings*** to subsequent recitations regarding the ***same elements*** (*i.e.*, the first plurality of registered chip select signals). In other words, the detailed obviousness analysis for limitation [15.5] for the combined Halbert Fig. 2 and Fig. 4 teachings also covered limitation [15.6] because the obviousness analysis for limitation [15.5] resulted in

the teachings of Halbert's Fig. 2 registered chip select signals being incorporated into Fig. 4, and limitation [15.6] is directed to using those same registered chip select signals of limitation [15.5] in the manner they normally operate.

Here, as in *KSR*, the patent claim is invalid as obvious because the element at issue is a feature "well within the grasp of a person of ordinary skill in the relevant art." *KSR*, 550 U.S. at 427. Accordingly, the Court should vacate the Board's decision.

C. The Board Erred in Inflexibly Requiring Micron to Demonstrate the Proposed Combination Works in All Modes of Halbert's Operation

The Court should likewise vacate the Board's determination because it improperly requires Micron to provide an explanation as to how the inactive select signal teaching would operate in Halbert's "concurrent ranks" mode. *See ParkerVision,* 903 F.3d at 1361 ("[A] prior art reference may anticipate or render obvious an apparatus claim—depending on the claim language—if the reference discloses an apparatus that is reasonably capable of operating so as to meet the claim limitations, even if it does not meet the claim limitations in all modes of operation[.]").

More specifically, the Board stated that "Halbert's Figure 5 shows ranks 140 and 142 operating ***concurrently*** to increase the throughput of the memory." Appx30

(emphasis added). The Board also recognized, however, that Halbert discloses a ***non-concurrent*** mode of operation:

> This is not to say that Halbert cannot be configured to operate with active and non-active signals such that ranks 140 and 142 do not operate concurrently. Indeed, Halbert discloses that "[*g*]*enerally*, multiple ranks will receive the same address and commands, and will perform memory operations with the interface circuit concurrently" (Ex. 1005 ¶ 30 (emphasis added)), which suggests that the memory need not be limited to concurrently-operating ranks.

Appx30. The Board discounted the non-concurrent mode on the basis that the non-concurrent mode would not allow for a specified data rate of "twice the data rate" of the ranks:

> Halbert's Figure 5 shows operating ranks 140 and 142 concurrently to increase memory throughput. If active and non-active signals are applied to ranks 140 and 142 in Halbert's Figure 5, the increased memory throughput would be eliminated by operating only one of the ranks at a time. In other words, Halbert's Figure 4 memory module would operate at the rate of each of ranks 140 and 142, rather than "twice the data rate" of the ranks.

Appx30-31. This determination was error for multiple reasons.

First, the Board had no basis for distinguishing Halbert based on a specified data rate. The challenged independent claims in the -745 proceeding (claims 15 and 28) do not recite a specified data rate. Appx2357-58, Appx2361-63. Nor did Micron argue that there was a motivation to combine because of a specified data rate. Appx2385-97. The Board's reference to a specified data rate has nothing to do with

the -745 Proceeding's challenged claims and cannot reasonably form the basis for a nonobviousness determination.

Second, the Board's obviousness test was again more rigid than *KSR* requires. Here, the Board required that Micron provide specific reasoning for "how Halbert's Figure 4 device would operate with active and non-active chip select signals" for the concurrent ranks operation, even though it was undisputed that Halbert also had a non-concurrent rank operation. Appx27. Under Halbert's select signal teachings, Halbert's non-concurrent operation would use active chip selects to select a rank and non-active chip selects to not select the other rank. Appx2396-97, Appx4037. The Board's rigid finding to the contrary "den[ies] factfinders recourse to common sense . . . [and is] neither necessary under [Supreme Court] case law nor consistent with it." *KSR*, 550 U.S. at 421.

This Court's precedent in *ParkerVision* is especially relevant here. The challenged claims here, just as in *ParkerVision*, are apparatus claims. And both this case and *ParkerVision* address whether the petitioner must provide specific analysis regarding how a proposed combination would operate, despite the fact that the claims are apparatus claims. The Court in *ParkerVision* held that the petitioner "was neither required to identify the conditions under which [the prior art] device will [operate in a specific way] nor obligated to explain why a person of skill in the art would have selected such operating conditions." *ParkerVision*, 903 F.3d at 1361.

The Court stated that "[w]e explained long ago that '[a]pparatus claims cover what a device is, not what a device does.'" *Id.* (quoting *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1468 (Fed. Cir. 1990)). Here, the Board's legal conclusion that the combined teachings of Halbert, as supported by Micron's apparatus-focused obviousness rationale, were not sufficient merely because Micron did not provide specific reasoning for each of Halbert's modes was legally wrong. Here, as in *ParkerVision*, Halbert "render[s] obvious" the "apparatus claim" because Halbert "discloses an apparatus that is reasonably capable of operating so as to meet the claim limitations, even if it does not meet the claim limitations in all modes of operation." *ParkerVision*, 903 F.3d at 1361.

Indeed, the facts here are more compelling than those in *ParkerVision* because Halbert implicitly discloses (i) a mode that would use active/active chip selects and (ii) another mode that would use active/non-active chip selects. More specifically, Halbert uses the conditional language of "generally" in describing accessing both memory ranks concurrently. *See* Appx3482 (¶30) ("Generally, multiple ranks will receive the same address and commands, and will perform memory operations with the interface circuit concurrently."). Through this statement, Halbert discloses a mode where communications with both ranks are active (the "general" operation) and implicitly discloses a non-concurrent mode where only one rank is active and the other is non-active. This express Halbert teaching of non-concurrent operations

cannot be squared with the Board's apparent requirement that Micron needed to "'explain why a [POSITA] would have combined elements from specific references *in the way the claimed invention does*,' accounting for the performance impact of not operating ranks 140 and 142 ***concurrently***." Appx31 (emphasis in original and added). *KSR* is not so inflexible that it ignores express modes of operation discussed in a single reference.

In light of the foregoing, the Board's obviousness conclusion was wrong as a matter of law. *KSR* and this Court's precedent confirm that the claim limitation reciting registered chip select signals that have active and non-active signal values is obvious, and as a result, the challenged claims are obvious. The Board's conclusion of nonobvious is therefore error, and the Court should vacate the Board's decision.

III. -745 IPR Proceeding: The Board Erred in Construing Limitations [15.6] and [28.6] [5]

For the -745 Decision, the Board also erred in construing the claims to require that non-active chip select signals be sent to the ranks. That requirement simply does not exist in the plain claim language. This Court reviews the Board's claim

[5] While the argument in this section focuses primarily on limitation 15.6, the argument applies equally to limitation 28.6.

construction of limitations [15.6] and [28.6] *de novo*. *See Personalized Media*, 952 F.3d at 1339.

More specifically, Micron identified that "the prior art registered chip select signals operation concepts described with respect to Figs. 2 and 3 could have been implemented in Fig. 4 in a variety of well-known and obvious ways." Appx4036-37. Micron further identified that "the use of active and non-active registered chip select signals could have been implemented with the MDQS signals and associated operations. . . . Therefore, the use of active and non-active chip select signals . . . could be used to trigger selecting DO_a1 from rank 140 (and not DO_a2 from rank 142) to be sent to buffer 122, while active and non-active chip select signals for ranks 142 and 140, respectively, are used a half-clock cycle later to send DO_a2 onto the memory bus." Appx4037. The Board incorrectly rejected these positions by determining that the claims require sending active/non-active chip select signals to the memory devices (ranks):

> Petitioner's argument falls short if the chip select signals are only used for selecting at the MUX/DeMUX because ***claims 15 and 28 recite that the memory devices are "configured to receive respective ones of the plurality of registered chip select signals***." ***If the active and non-active signals are only used at the MUX/DeMUX and are not sent to the memory devices (ranks 140 and 142),*** then the combination does not show memories that are "configured to receive respective ones of the plurality of registered chip select signals."

Appx32 (emphasis added).

The Board's error is manifest. Claims 15 and 28 do indeed recite "ranks are configured to receive respective ones of the [first] plurality of registered chip select signals." Appx2357, Appx2362. Unlike claim 1 challenged in the -744 Proceeding, however, independent claims 15 and 28 do not recite that non-active chip select signals are sent to the ranks. Appx2357-58, Appx2361-63. Claims 15 and 28 only recite "a first N-bit wide rank [in the plurality of N-bit wide ranks] receiving the [first] registered chip select signal having the active signal value" (Appx2358, Appx2362) and do not place limitations on the non-active signals being sent to a memory device, rank, or a MUX/DeMUX.

While the Board generally stated, "[w]e need not construe expressly any claim terms to decide the issues before us" (Appx21), the Board applied specific claim constructions to claim limitations [15.6] and [28.6] in reaching its decision. The Board consistently reiterated its finding that the claims require that both the "active and non-active chip select signals" be applied (or sent) to the memory devices (ranks 140 and 142):

> Petitioner's argument . . . is misplaced because the combined teachings do not suggest the subject matter of recitation 15.6. That is, Petitioner has not provided adequate reasoning to ***apply active and non-active chip select signals to ranks 140 and 142***, as discussed above.

Appx33 (emphasis added).

> If ***active and non-active signals are applied to ranks 140 and 142*** in Halbert's Figure 5, the increased memory

> throughput would be eliminated by operating only one of the ranks at a time. . . . Petitioner's analysis for limitation 15.6 does not sufficiently address Halbert's Figure 4, . . . accounting for the performance impact of not operating ranks 140 and 142 concurrently.

Appx30-31 (emphasis added).

The Board's foregoing discussion regarding the meaning and requirements of claims 15 and 28 make clear that the Board engaged in claim construction. *See Google*, 92 F.4th at 1055-56 (holding that "the Board's assessment of the [1m] limitation amounts to claim construction" and noting that "the Board's statement that it was not engaging in claim construction is not dispositive as to whether claim construction occurred").

The Board erred in construing the claims to require applying non-active chip select signals to the ranks. Claims are construed according to their plain and ordinary meaning absent lexicography or clear disavowal. *Golden Bridge*, 758 F.3d at 1365. No lexicography or disavowal exists, and the plain meaning applies. The Board's construction requiring more was therefore erroneous. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1314 (Fed. Cir. 2005) ("In some cases, the ordinary meaning of claim language as understood by a person of skill in the art may be readily apparent even to lay judges, and claim construction in such cases involves little more than the application of the widely accepted meaning of commonly understood words.").

In sum, the Board erred in construing claims 15 and 28 as requiring that both the "active and non-active chip select signals" be applied (or sent) to the memory devices (ranks 140 and 142). Accordingly, this Court should vacate the Board's construction and remand for a proper claim construction determination.

CONCLUSION

For the reasons discussed above, the Court should vacate the Board's decisions and remand.

Respectfully submitted,

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June 26, 2024

ADDENDUM

TABLE OF CONTENTS

Trials@uspto.gov
571-272-7822

Paper 34
Date: October 30, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR PRODUCTS, INC., and
MICRON TECHNOLOGY TEXAS LLC,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00744
Patent 10,489,314 B2

Before PATRICK M. BOUCHER, JON M. JURGOVAN, and DANIEL J. GALLIGAN, *Administrative Patent Judges.*

GALLIGAN, *Administrative Patent Judge.*

JUDGMENT
Final Written Decision
Determining No Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

In this *inter partes* review, Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC (collectively "Petitioner") challenge the patentability of claims 1–3, 5, 6, 8–10, and 12–14 of U.S. Patent No. 10,489,314 B2 (Ex. 1001, "the '314 patent"), which is assigned to Netlist, Inc. ("Patent Owner").

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision, issued pursuant to 35 U.S.C. § 318(a), addresses issues and arguments raised during the trial in this *inter partes* review. For the reasons discussed below, we determine that Petitioner has not proven by a preponderance of the evidence that claims 1–3, 5, 6, 8–10, and 12–14 of the '314 patent are unpatentable. *See* 35 U.S.C. § 316(e) (2018) ("In an inter partes review instituted under this chapter, the petitioner shall have the burden of proving a proposition of unpatentability by a preponderance of the evidence.").

A. Procedural History

Petitioner filed a Petition (Paper 2, "Pet.") challenging claims 1–3, 5, 6, 8–10, and 12–14 of the '314 patent on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1, 2, 6, 8, 12–14	103(a)[1]	Halbert[2]
3, 9, 10	103(a)	Halbert, JESD21-C[3]
5	103(a)	Halbert, JESD79-2A[4]

[1] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103 and became effective March 16, 2013. Petitioner applies the pre-AIA version of § 103. Pet. 2–3.
[2] Ex. 1005, US 2002/0112119 A1, published Aug. 15, 2002.
[3] Ex. 1006, PC2100 and PC1600 DDR SDRAM Registered DIMM Design Specification, JEDEC Standard 21-C (January 2002).
[4] Ex. 1007, DDR2 SDRAM Specification, JESD79-2A (January 2004).

Pet. 2–3. Patent Owner filed a Preliminary Response. Paper 9. As authorized, Petitioner filed a preliminary reply (Paper 11), and Patent Owner filed a preliminary sur-reply (Paper 12). Trial was instituted on the asserted grounds of unpatentability. Paper 15 ("Inst. Dec."), 22.

During the trial, Patent Owner filed a Response (Paper 19, "PO Resp."), Petitioner filed a Reply (Paper 25, "Pet. Reply"), and Patent Owner filed a Sur-reply (Paper 26, "PO Sur-reply").

An oral hearing was held on August 15, 2023, a transcript of which appears in the record. Paper 33.

Petitioner relies on testimony from Dr. Vojin Oklobdzija. Ex. 1003. Patent Owner relies on testimony from Dr. Steven Przybylski. Ex. 2003. The parties have entered in the record transcripts for depositions of these declarants. Exs. 1013, 2004.

B. Real Parties in Interest

The parties identify themselves as the real parties in interest. Pet. 82; Paper 3, 1.

C. Related Matters

As required by 37 C.F.R. § 42.8(b)(2), the parties identify various related matters, including IPR2022-00745, in which we are issuing a final written decision concurrently with this Decision. Pet. 82; Paper 3, 1.

D. Illustrative Claim

The '314 patent is titled "Memory Module with Data Buffering." Ex. 1001, code (54). Independent claim 1 is reproduced below.

> 1. A memory module operable in a computer system to communicate data with a memory controller of the computer system at a specified data rate via a N-bit wide data bus in response to memory commands received from the memory controller, the memory commands including a first memory

command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first burst of N-bit wide data signals and a first burst of data strobes and the second memory command to cause the memory module to receive or output a second burst of N-bit wide data signals and a second burst of data strobes, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, wherein the plurality of N-bit wide ranks include a first rank configured to receive or output the first burst of N-bit wide data signals and the first burst of data strobes at the specified data rate in response to the first memory command, and a second rank configured to receive or output the second burst of N-bit wide data signals and the second burst of data strobes at the specified data rate in response to the second memory command;

circuitry coupled between the plurality of N-bit wide ranks and the N-bit wide data bus; and

logic coupled to the circuitry and configured to respond to the first memory command by providing first control signals to the circuitry and to subsequently respond to the second memory command by providing second control signals to the circuitry, wherein the circuitry is configured to enable data transfers through the circuitry in response to the first control signals and subsequently in response to the second control signals, wherein respective N-bit wide data signals of the first burst of N-bit wide data signals and respective data strobes of the first burst of data strobes are transferred at the specified data rate between the first rank and the N-bit wide data bus through the circuitry, and wherein respective N-bit wide data signals of the second burst of N-bit wide data signals and respective data strobes of the second burst of data strobes are transferred at the specified data rate between the second rank and the N-bit wide data bus through the circuitry;

> wherein the data transfers through the circuitry are registered data transfers enabled in accordance with an overall CAS latency of the memory module, and the circuitry is configured to add a predetermined amount of time delay for each registered data transfer through the circuitry so that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the plurality of memory integrated circuits.

II. ANALYSIS

A. Principles of Law

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) any secondary considerations, if in evidence. *Graham v. John Deere Co. of Kan. City*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art "would have been someone with an advanced degree in electrical or computer engineering and at least two years working in the field, or a bachelor's degree in such engineering disciplines and at least three years working the field," and Petitioner identifies particular knowledge that a person of ordinary skill in the art would have had. Pet. 3–4 (citing Ex. 1003 ¶ 52).

At institution, Petitioner's proposed skill level was adopted, with the exception of the phrases "at least." Inst. Dec. 11.

Patent Owner does not provide a different assessment of the level of ordinary skill, but Dr. Przybylski states that an individual with the level of experience identified by Petitioner "would have less knowledge and familiarity" than presumed by Petitioner's definition. Ex. 2003 ¶ 46. Dr. Przybylski, however, provides no further discussion explaining this apparent disagreement with Petitioner, nor does he set forth what level of knowledge and familiarity a person of ordinary skill in the art would have had.

Based on the complete trial record, we determine that Petitioner's proposed skill level is consistent with the level of ordinary skill evidenced by the '314 patent and the asserted prior art, and we adopt that skill level with the exception of the phrases "at least," which introduce vagueness as to the amount of experience.

C. Claim Construction

The dispositive issue in this case implicates the meaning of the phrase "specified data rate" in claim 1. The preamble of claim 1 recites, in relevant part, a "memory module operable in a computer system to communicate data with a memory controller of the computer system at a specified data rate." Claim 1 recites "specified data rate" four more times, including in the following limitation:

> a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, wherein the plurality of N-bit wide ranks include a first rank configured to receive or output the first burst of N-bit wide data signals and the first burst of data strobes *at the specified data rate* in response to the first memory command, and a second rank configured to receive or output the second burst of N-bit wide

> data signals and the second burst of data strobes *at the specified data rate* in response to the second memory command

(emphases added).

Patent Owner argues that the instances of "the specified data rate" in the body of claim 1 refer to the "specified data rate" that is introduced in the preamble of claim 1. PO Resp. 15. According to Patent Owner, therefore, "claim 1 recites that the ***same specified data rate*** is used when transferring information between the ranks and memory controller of the computer system." PO Resp. 17.

Petitioner "do[es] not dispute whether claim 1's preamble is limiting and agree[s] that 'a specified data rate' in the preamble provides antecedent basis for 'the specified data rate' recited in the remainder of the claim." Pet. Reply 2; *see also* Pet. Reply 4 ("Again, Petitioner[] do[es] not dispute that the term 'the specified data rate' throughout claim 1 refers to 'a specified data rate' in the preamble."). Petitioner, however, argues that "'a specified data rate' is not limited to a single numerical value." Pet. Reply 4. Petitioner argues that "Patent Owner has pointed to no evidence—intrinsic or extrinsic—that requires limiting 'specified data rate' to a single numerical value." Pet. Reply 2.

We disagree with Petitioner's interpretation. Taking Petitioner's point that "'specified data rate' means only that the data rate is specified in some way" (Pet. Reply 4), we do not see how, once the rate is specified, claim 1's later recitations of "the specified data rate" could refer to any other rate, as Petitioner's arguments suggest. Petitioner argues that "it is clear that the 'specified data rate' that provides antecedent basis for later recitations of that term is merely the data rate specified for 'communicat[ing] data' between the 'memory module' and the external 'memory controller of the computer

system,' as expressly recited in the preamble of claim 1." Pet. Reply 3 (alteration by Petitioner). We agree with this statement, and later recitations of "the specified data rate," therefore, refer to the data rate that is so specified. Petitioner provides no persuasive argument to support its position that later recitations of "the specified data rate" could be satisfied by data rates that are not the "specified data rate."

Petitioner asserts that, "[i]f the data rate was intended to be limited to a single numerical value, the patentee would have just claimed '[a/the] data rate' throughout the claim." Pet. Reply 4 (second set of brackets added by Petitioner). In other words, Petitioner argues that the word "specified" means that the multiple occurrences of the "data rate" in the claim are not limited to a single numerical value. Pet. Reply 4.

We do not agree with Petitioner that the phrase "the data rate" is any more specific than "the specified data rate" or that the use of the qualifier "specified" broadens the claim to encompass multiple values. Although Petitioner posits that the applicant could have used different language to limit the rate to a single numerical value (Pet. Reply 4), the applicant also could have recited different terms for different instances of "rate," such as "a first specified data rate" and a "a second specified data rate" to clearly convey such a meaning.

We determine that the plain language of claim 1 requires that later recitations of "the specified data rate" refer to the same data rate as "a specified data rate" in the preamble, which is the rate at which data are communicated between the memory module and the memory controller.

We need not construe expressly any other claim terms to decide the issues before us. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) ("The Board is required to construe 'only those terms . . .

that are in controversy, and only to the extent necessary to resolve the controversy.'" (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

D. Obviousness over Halbert (Claims 1, 2, 6, 8, 12–14)

Petitioner asserts that claims 1, 2, 6, 8, and 12–14 would have been obvious over the teachings of Halbert. Pet. 17–44. Patent Owner opposes. PO Resp. 12–49; PO Sur-reply 1–18.

Claim 1 recites "[a] memory module operable in a computer system to communicate data with a memory controller of the computer system at a specified data rate" and then recites

> a plurality of memory integrated circuits . . . arranged in a plurality of N-bit wide ranks, wherein the plurality of N-bit wide ranks include a first rank configured to receive or output the first burst of N-bit wide data signals and the first burst of data strobes *at the specified data rate* in response to the first memory command, and a second rank configured to receive or output the second burst of N-bit wide data signals and the second burst of data strobes *at the specified data rate* in response to the second memory command

(emphases added). As discussed above in § II.C, claim 1's later recitations of "the specified data rate" refer to the same data rate as "a specified data rate" in the preamble. Thus, claim 1 requires "a first rank configured to receive or output the first burst of N-bit wide data signals and the first burst of data strobes at" the same rate at which data are communicated between the memory module and the memory controller. Similarly, claim 1 requires "a second rank configured to receive or output the second burst of N-bit wide data signals and the second burst of data strobes at" this same data rate. As explained below, Petitioner's contentions do not show this.

Petitioner's contentions refer to Halbert's Figure 4, reproduced below.

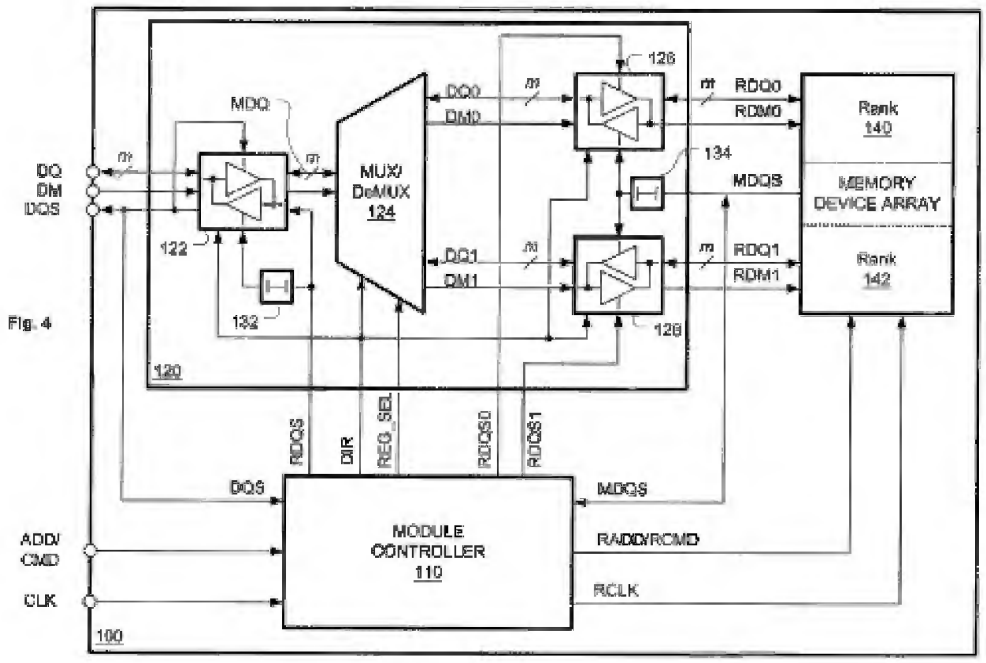


Fig. 4

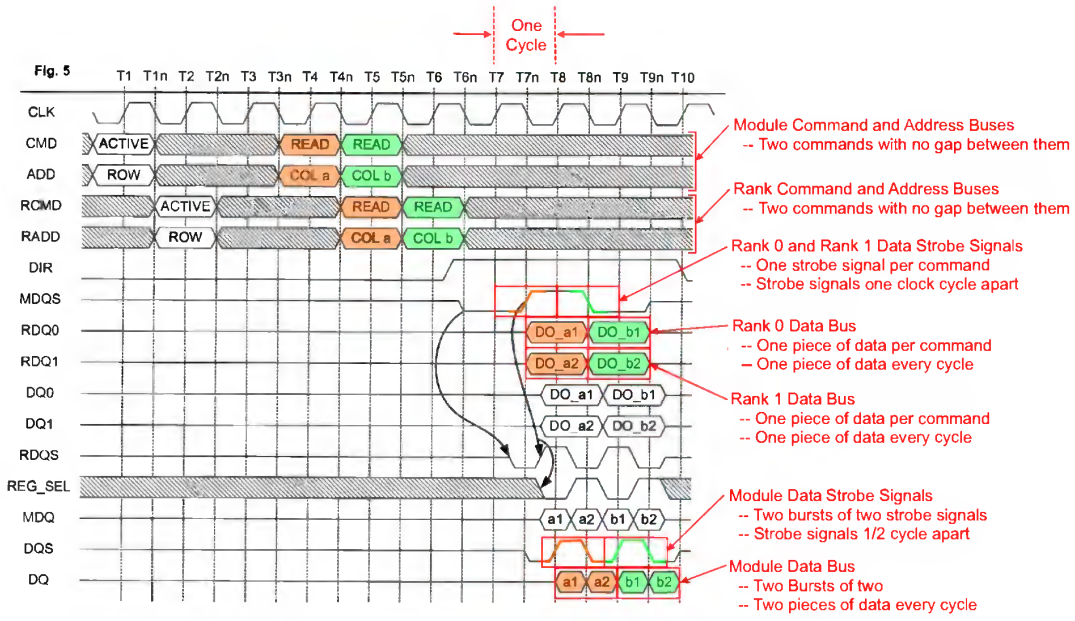
Halbert's Figure 4 illustrates memory module 100 having memory device ranks 140 and 142. Ex. 1005 ¶¶ 27, 30. Petitioner identifies ranks 140 and 142 as, respectively, "a first rank" and "a second rank," as recited in claim 1. Pet. 22–24. Petitioner argues the following:

> Memory module 100 has a data interface circuit 120 that "provides for m-bit-wide data transfers between the module and the system memory data bus, and for R×m-bit-wide data transfers between the interface circuit and the memory device array. In FIG. 4, R=2, i.e., the memory device array comprises two memory device ranks 140 and 142."

Pet. 18 (quoting Ex. 1005 ¶ 30). Thus, the "specified data rate" is the rate at which data are communicated between data interface circuit 120 and the system memory data bus over the m-bit wide line to output labeled "DQ" on the left side of Figure 4 above. As Patent Owner correctly points out, however, each of Halbert's ranks 140 and 142 receives and outputs data at

half the rate as data are communicated between the memory module and system memory bus, as explained below. *See* PO Resp. 12–28.

Patent Owner provides the annotated version of Halbert's Figure 5 below.



PO Resp. 19; *see also* Ex. 2003 ¶¶ 68–72 (Dr. Przybylski's testimony explaining this annotated figure). Halbert's Figure 5 is a timing diagram for two consecutive read operations (Ex. 1005 ¶¶ 16, 37), and Patent Owner includes annotations to show each of ranks 140 and 142 outputting data onto their respective data busses at half the rate that data are output from data interface circuit 120 on the DQ data line.

In particular, Halbert explains that each of ranks 140 and 142 is "capable of performing m-bit-wide data transfers." Ex. 1005 ¶ 30. On a read command, rank 140 sends m-bit-wide data to bi-directional data register 126 on line RDQ0 at the same time that rank 142 sends m-bit-wide data to bi-directional data register 128 on line RDQ1, as shown in Figure 5 between T7n and T8n. Ex. 1005 ¶¶ 31–32, 39. Halbert discloses that

multiplexer/demultiplexer (MUX/DeMUX) 124 selects data from either register 126 or from register 128 to output to buffer 122, which are then output on line DQ. Ex. 1005 ¶ 33. Halbert explains that "[d]ata is serialized from the data registers onto the memory data bus by reading 2m bits into the data registers during one memory device read cycle, and then driving these bits, m at a time, through MUX 124." Ex. 1005 ¶ 33. As shown in Halbert's Figure 5, over one clock cycle (T7n–T8n), each of ranks 140 and 142 outputs one piece of m-bit-wide data, and over one clock cycle (T8–T9), those two pieces of m-bit-wide data are output on line DQ to the system memory data bus. Halbert explains that the second read operation proceeds in the same fashion as the first and that "[t]he net result is that the memory data bus transfers 4m bits of data in two memory bus clock cycles (four m-bit transfers), with only two data accesses performed at each memory device on the module." Ex. 1005 ¶ 42. Thus, Halbert's memory module outputs data to the system memory data bus at twice the rate that each of ranks 140 and 142 outputs data. *See* Ex. 2003 ¶¶ 68–73 (Dr. Przybylski's credible testimony explaining Halbert's data rates).

We disagree with Petitioner's argument in the Reply that "Halbert still renders the 'specified data rate' limitations obvious even under" the construction we adopt above. *See* Pet. Reply 4–5. In particular, Petitioner argues the following:

> The DQ0 data associated with memory device array rank 140 is clocked out by REG_SEL (Ex. 1005, [0035]), which is at the "specified data rate" because it has the same clock rate as the DQS clock rate that clocks the DQ data out of the memory module to the memory controller. Resp. 25. This includes transfer through the circuitry (data interface circuit 120) because as shown in Fig. 5, data is output from DQ0 onto MDQ in data interface circuit 120 at one burst of data per half clock cycle and

> out of the data interface circuit 120 onto DQ also at one burst of data per half clock cycle. Thus, because the REG_SEL signal clocks the DQ0 data between memory device array rank 140 and the data interface circuit 120 (and through data interface circuit 120) at the same clock rate that is used to clock the DQ data between the data interface circuit 120 and the memory module external connections, Halbert discloses or renders obvious the "specified data rate" limitations even under Patent Owner's incorrect interpretation of the "specified data rate" limitations.

Pet. Reply 5. Petitioner's argument does not show that each of ranks 140 and 142 is configured to receive or output data at the specified data rate. Rather, the REG_SEL signal controls MUX/DeMUX 24 to determine whether DQ0 or DQ1 data are passed through to buffer 122 and ultimately out of memory module 100 on a read command. Ex. 1005 ¶ 35. Halbert explains that "Multiplexer/demultiplexer (MUX/DeMUX) 124 has a multiplexing ratio R," which is 2 in Figure 4 because there are two ranks. Ex. 1005 ¶¶ 30, 33. Thus, MUX/DeMUX 24 is what allows selection of data between each of ranks 140 and 142, thereby allowing the memory module to operate at twice the rate of each of the ranks. *See, e.g.*, Ex. 1005 ¶ 23 ("Generally, the disclosed embodiments use a memory module interface circuit that, in essence, widens the data bus on the memory module as compared to the width of the system memory data bus, allowing a faster system memory data bus to operate at full speed with slower memory devices.").

Based on the foregoing, we determine Petitioner has not shown that Halbert teaches that each of the first and second ranks communicates data at the specified data rate, which is the rate at which data are communicated between the memory module and the system memory bus, as we construe the term above in § II.C.

Based on the complete trial record, we determine that Petitioner fails to show by preponderant evidence that claim 1 would have been obvious based on Halbert. Petitioner's contentions for claims 2, 3, 5, 6, 8–10, and 12–14, which depend directly or indirectly from claim 1, do not remedy the deficiencies discussed above and, therefore, also fail to show unpatentability.

III. CONCLUSION

For the reasons discussed above, we determine that Petitioner has not proven, by a preponderance of the evidence, that claims 1–3, 5, 6, 8–10, and 12–14 of the '314 patent are unpatentable, as summarized in the following table:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
1, 2, 6, 8, 12–14	103(a)	Halbert		1, 2, 6, 8, 12–14
3, 9, 10	103(a)	Halbert, JESD21-C		3, 9, 10
5	103(a)	Halbert, JESD79-2A		5
Overall Outcome				1–3, 5, 6, 8–10, 12–14

IV. ORDER

Accordingly, it is

ORDERED that claims 1–3, 5, 6, 8–10, and 12–14 of the '314 patent have not been shown to be unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2022-00744
Patent 10,489,314 B2

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Paper 34
Date: October 30, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR PRODUCTS, INC., and
MICRON TECHNOLOGY TEXAS LLC,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00745
Patent 10,489,314 B2

Before PATRICK M. BOUCHER, JON M. JURGOVAN, and DANIEL J. GALLIGAN, *Administrative Patent Judges.*

GALLIGAN, *Administrative Patent Judge.*

JUDGMENT
Final Written Decision
Determining No Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

In this *inter partes* review, Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC (collectively "Petitioner") challenge the patentability of claims 15–20 and 22–33 of U.S. Patent No. 10,489,314 B2 (Ex. 1001, "the '314 patent"), which is assigned to Netlist, Inc. ("Patent Owner").

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision, issued pursuant to 35 U.S.C. § 318(a), addresses issues and arguments raised during the trial in this *inter partes* review. For the reasons discussed below, we determine that Petitioner has not proven by a preponderance of the evidence that claims 15–20 and 22–33 of the '314 patent are unpatentable. *See* 35 U.S.C. § 316(e) (2018) ("In an inter partes review instituted under this chapter, the petitioner shall have the burden of proving a proposition of unpatentability by a preponderance of the evidence.").

A. Procedural History

Petitioner filed a Petition (Paper 2, "Pet.") challenging claims 15–20 and 22–33 of the '314 patent on the following ground:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
15–20, 22–33	103(a)[1]	Halbert,[2] JESD21-C[3]

Pet. 2–3. Patent Owner filed a Preliminary Response. Paper 9. As authorized, Petitioner filed a preliminary reply (Paper 11), and Patent Owner

[1] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103 and became effective March 16, 2013. Petitioner applies the pre-AIA version of § 103. Pet. 2–3.
[2] Ex. 1005, US 2002/0112119 A1, published Aug. 15, 2002.
[3] Ex. 1006, PC2100 and PC1600 DDR SDRAM Registered DIMM Design Specification, JEDEC Standard 21-C (January 2002).

filed a preliminary sur-reply (Paper 12). Trial was instituted on the asserted ground of unpatentability. Paper 15 ("Inst. Dec."), 27.

During the trial, Patent Owner filed a Response (Paper 19, "PO Resp."), Petitioner filed a Reply (Paper 25, "Pet. Reply"), and Patent Owner filed a Sur-reply (Paper 26, "PO Sur-reply").

An oral hearing was held on August 15, 2023, a transcript of which appears in the record. Paper 33.

Petitioner relies on testimony from Dr. Vojin Oklobdzija. Ex. 1003. Patent Owner relies on testimony from Dr. Steven Przybylski. Ex. 2003. The parties have entered in the record transcripts for depositions of these declarants. Exs. 1013, 2004.

B. Real Parties in Interest

The parties identify themselves as the real parties in interest. Pet. 90; Paper 3, 1.

C. Related Matters

As required by 37 C.F.R. § 42.8(b)(2), the parties identify various related matters, including IPR2022-00744, in which we are issuing a final written decision concurrently with this Decision. Pet. 90; Paper 3, 1.

D. Illustrative Claim

The '314 patent is titled "Memory Module with Data Buffering." Ex. 1001, code (54). Independent claim 15 is reproduced below.

> 15. A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller, the memory module comprising:
>
> a printed circuit board having a plurality of edge connections configured to be electrically coupled to a

corresponding plurality of contacts of a module slot of the computer system;

logic coupled to the printed circuit board and configured to receive a first set of input address and control signals associated with a first read or write memory command and to output a first set of registered address and control signals in response to the first set of input address and control signals, the first set of input address and control signals including a first plurality of input chip select signals, the first set of registered address and control signals including a first plurality of registered chip select signals corresponding to respective ones of the first plurality of input chip select signals, the first plurality of registered chip select signals including a first registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value;

memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, wherein the plurality of N-bit wide ranks are configured to receive respective ones of the first plurality of registered chip select signals, wherein a first N-bit wide rank in the plurality of N-bit wide ranks receiving the first registered chip select signal having the active signal value is configured to receive or output a first burst of N-bit wide data signals and a first burst of data strobes associated with the first read or write command;

circuitry coupled between data and strobe signal lines in the N-bit wide memory bus and corresponding data and strobe pins of memory devices in each of the plurality of N-bit wide ranks; and

wherein the logic is further configured to, in response to the first read or write memory command, output first control signals to the circuitry, and wherein the circuitry is configured to enable data transfers between the first rank and the memory bus through the circuitry in response to the first control signals so that respective N-bit wide data signals of the first burst of N-bit wide data signals and respective data strobes of the first burst of data strobes are transferred through the circuitry in accordance with an overall CAS latency of the memory module; and

> wherein the data transfers between the first rank and the memory bus through the circuitry are registered data transfers and the circuitry is configured to add a predetermined amount of time delay for each registered data transfer through the circuitry such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.

II. ANALYSIS

A. Principles of Law

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) any secondary considerations, if in evidence. *Graham v. John Deere Co. of Kan. City*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art "would have been someone with an advanced degree in electrical or computer engineering and at least two years working in the field, or a bachelor's degree in such engineering disciplines and at least three years working the field," and Petitioner identifies particular knowledge that a person of ordinary skill in the art would have had. Pet. 3–4 (citing Ex. 1003 ¶ 52).

At institution, Petitioner's proposed skill level was adopted, with the exception of the phrases "at least." Inst. Dec. 12.

Patent Owner does not provide a different assessment of the level of ordinary skill, but Dr. Przybylski states that an individual with the level of experience identified by Petitioner "would have less knowledge and familiarity" than presumed by Petitioner's definition. Ex. 2003 ¶ 46. Dr. Przybylski, however, provides no further discussion explaining this apparent disagreement with Petitioner, nor does he set forth what level of knowledge and familiarity a person of ordinary skill in the art would have had.

Based on the complete trial record, we determine that Petitioner's proposed skill level is consistent with the level of ordinary skill evidenced by the '314 patent and the asserted prior art, and we adopt that skill level with the exception of the phrases "at least," which introduce vagueness as to the amount of experience.

C. Claim Construction

We need not construe expressly any claim terms to decide the issues before us. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) ("The Board is required to construe 'only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.'" (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

D. Obviousness over Halbert and JESD21-C (Claims 15–20, 22–33)

Petitioner asserts that claims 15–20 and 22–33 would have been obvious over the combined teachings of Halbert and JESD21-C. Pet. 15–84. Patent Owner argues that the claims are not unpatentable. PO Resp. 12–52;

PO Sur-reply 1–25. For the reasons discussed below, we determine that Petitioner's contentions do not show that claims 15–20 and 22–33 are unpatentable over the asserted ground.

> Independent claim 15 recites a memory module comprising
>
> [15.3] logic . . . configured to receive a first set of input address and control signals associated with a first read or write memory command and to output a first set of registered address and control signals in response to the first set of input address and control signals, [15.4] the first set of input address and control signals including a first plurality of input chip select signals, [15.5] the first set of registered address and control signals including a first plurality of registered chip select signals corresponding to respective ones of the first plurality of input chip select signals, [15.6] *the first plurality of registered chip select signals including a first registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value*

(emphasis added; Petitioner's limitation identifiers in brackets (*see* Pet. x)). Independent claim 28 is directed to a memory module having similarly recited logic, including the active and non-active signal value subject matter emphasized above. Petitioner relies on the same arguments for this subject matter in both claims. *See* Pet. 78 (for claim 28, referring to claim 15).

For the teaching of a memory module, Petitioner identifies Halbert's memory module 100 in Figure 4, reproduced below. Pet. 15–16.

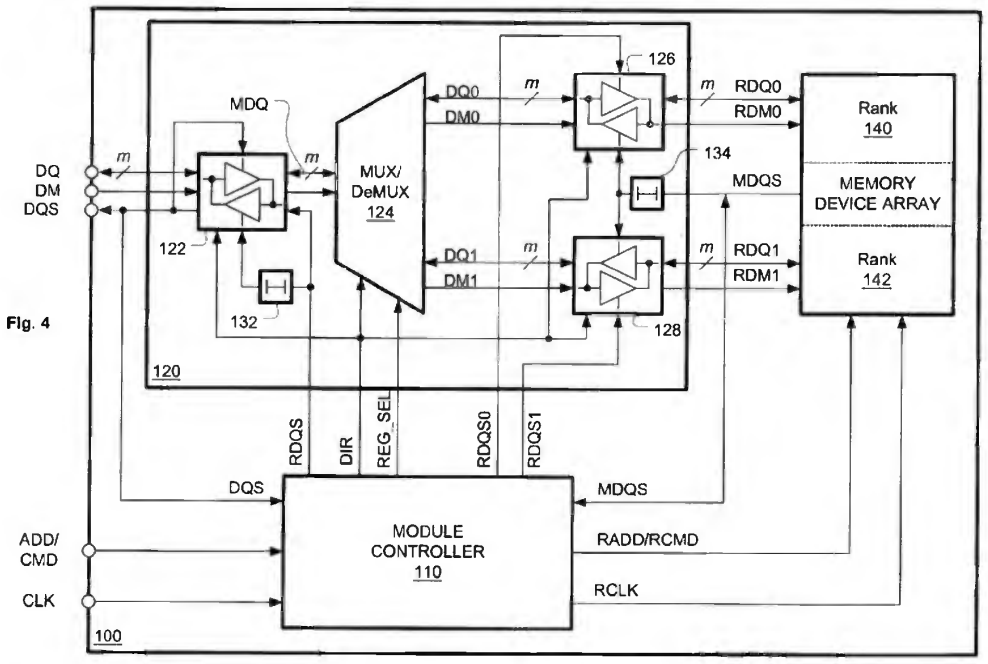


Fig. 4

Halbert's Figure 4 is a block diagram of memory module 100 including memory ranks 140 and 142, module controller 110, and data interface circuit 120. Ex. 1005 ¶¶ 27–28. Petitioner argues that Halbert's disclosure of module controller 110 teaches recitation 15.3. Pet. 18–19.

For recitation 15.4 ("the first set of input address and control signals including a first plurality of input chip select signals"), Petitioner relies on Halbert's disclosure of bank select signals B0_SEL# and B1_SEL# in Halbert's Figure 2 to teach chip select signals and argues that it would have been obvious to include those bank select signals in Halbert's Figure 4 memory module "to select whether data is transferred to/from memory device rank 140 or 142." Pet. 20–22 (citing Ex. 1005 ¶¶ 9, 37, Figs. 2, 4; Ex. 1003 ¶¶ 244–245).

Alternatively, Petitioner relies on JESD21-C for teaching a first plurality of input chip select signals S0 and S1 as shown in the Raw Card Version N diagram in JESD21-C. Pet. 22–23 (citing Ex. 1006, 15; Ex. 1003

¶ 146). Petitioner argues that the Card N block diagram shows two physical banks of SDRAM and that chip select S0 corresponds to the bank that includes D0–D17 memory devices, while chip select S1 corresponds to the bank that includes D18–D35 memory devices. Pet. 22–23 (citing Ex. 1006, 15; Ex. 1003 ¶ 246). According to Petitioner, this is similar to what is disclosed in Figure 4 of Halbert where there are memory devices in two ranks—ranks 140 and 142. Pet. 23. Petitioner argues that both references are in the same field and are directed toward improving the design of memory modules using SDRAM. Pet. 23–24 (citing Ex. 1003 ¶ 247). Petitioner argues that one of ordinary skill would have been motivated to design the memory modules of Halbert to comply with an industry wide standard such as JEDEC. Pet. 24 (citing Ex. 1003 ¶ 247). Further, according to Petitioner, one of ordinary skill would have been motivated to combine JESDC-21C with Halbert because Halbert's goal is to improve on dual-bank registered DIMMs and JESD21-C is a specification that defines registered DDR SDRAM DIMMs. Pet. 24 (citing Ex. 1003 ¶ 247).

For recitation 15.5 ("the first set of registered address and control signals including a first plurality of registered chip select signals corresponding to respective ones of the first plurality of input chip select signals"), Petitioner identifies RB0_SEL# and RB1_SEL# in Halbert's Figure 2 as registered chip select signals. Pet. 27–28 (citing Ex. 1005 ¶ 9, Fig. 2; Ex. 1003 ¶ 251). Petitioner argues that, in the proposed combination in which chip select signals are implemented in Halbert's Figure 4, module controller 110 "would have a plurality of registered chip selects as outputs because there are multiple memory device ranks 140 and 142, and there would be registered chip selects to select whether data is transferred to/from memory device rank 140 or 142." Pet. 28–29 (citing Ex. 1005, Fig. 4;

Ex. 1003 ¶ 252); *see also* Pet. 29–31 (similarly asserting for the combination of Halbert and JESD21-C "there would [be] a first plurality of registered chip selects output from module controller 110 in Fig. 4 that correspond to the first plurality of input chip select signals").

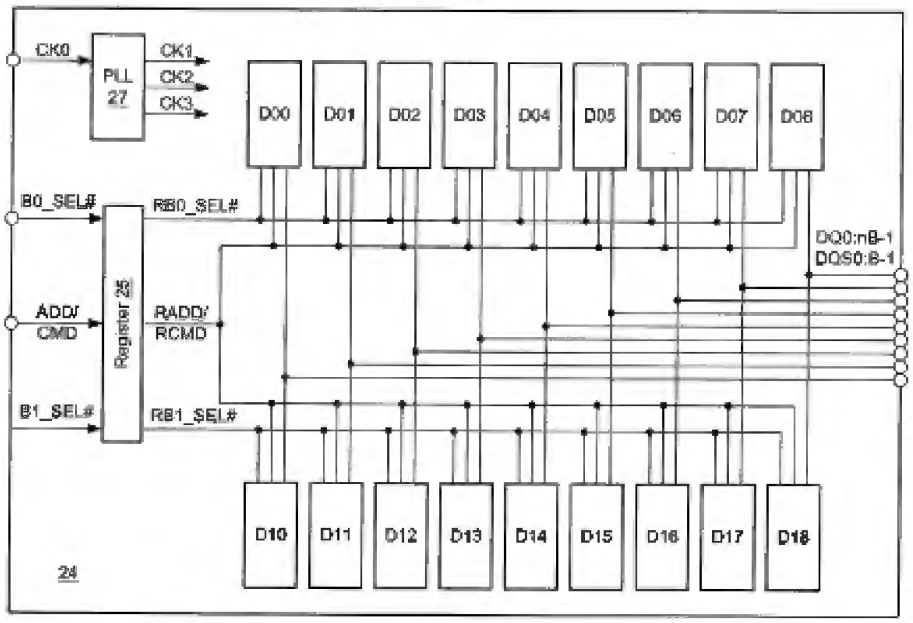
For recitation 15.6 ("the first plurality of registered chip select signals including a first registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value"), Petitioner argues the following:

> Halbert discloses Limitation [15.6]. As discussed above, Halbert discloses a first plurality of registered chip select signals RB0_SEL# and RB1_SEL#. Referring to Fig. 2 below, RB0_SEL# has an active signal value when selecting the D00-D08 memory ranks for data transfers. When RB0_SEL# has an active signal value, RB1_SEL# has a non-active signal value because the D10-D18 memory ranks are not selected for data transfers. . . .
>
> RB0_SEL# having an active signal value while RB1_SEL# has a non-active signal value is reflected in Fig. 3 below. . . . As shown in Fig. 3, RB0_SEL# is low to indicate that it has an active signal value at all times the registered address and control signals are active, while RB1_SEL# is high to indicate that it has a non-active signal value during those times.

Pet. 31–32 (citing Ex. 1005, Figs. 2, 3; Ex. 1003 ¶¶ 255–256).

Thus, Petitioner relies on Halbert's Figure 2 prior art embodiment for the subject matter of claim 15 reciting active and non-active chip select signals. *See* Pet. 31–32. Halbert's Figure 2 is reproduced below.

Fig. 2
(Prior Art)



Halbert's Figure 2 is a block diagram of registered Dual In-Line Memory Module (DIMM) 24 having two banks of memory, one bank having memory devices D00–D08 and the other bank having memory devices D10–D18. Ex. 1005 ¶ 9. Registered bank select signals RB0_SEL# and RB1_SEL# control, respectively, banks D00–D08 and D10–D18. Ex. 1005 ¶¶ 9–10, Fig. 2; *see* Pet. 31 (explaining that RB0_SEL# is active to select D00–D08 while RB1_SEL# is inactive).

Patent Owner argues that Petitioner failed to meet its burden with respect to recitation 15.6. PO Resp. 12–22. In particular, Patent Owner argues that "Petitioners provide no obviousness analysis *at all* relating to" recitation 15.6 and instead rely only on Halbert's Figure 2 prior art disclosures. PO Resp. 12–13.

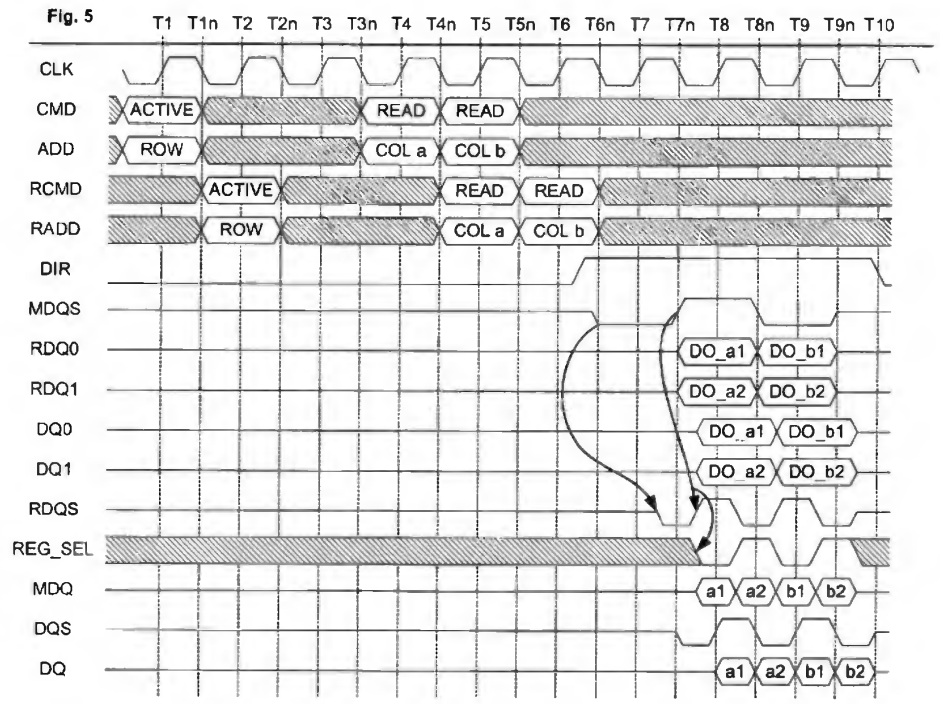
Petitioner counters that its contentions for recitation 15.5 already explain why a person of ordinary skill in the art "would have included

registered chip select signals in Fig. 4." Pet. Reply 2. Petitioner asserts that recitation 15.6 "directly relates to how registered chip select signals normally function" and, therefore, that "no additional obviousness analysis for" this subject matter "is required because the teachings of registered chip select signals have already been incorporated into Fig. 4, and Limitation [15.6] is directed to using the registered chip select signals in the manner they normally operate, as illustrated in Halbert's Fig. 3." Pet. Reply 2–3.

For the reasons explained below, we agree with Patent Owner that Petitioner's assertions for limitation 15.6 are inadequate.

As outlined above, Petitioner presents reasoning as to why a person of ordinary skill in the art would have included chip select signals in Halbert's Figure 4 device. *See* Pet. 20–31 (addressing limitations 15.4 and 15.5). But Petitioner's contentions about the use of chip select signals do not address sufficiently how Halbert's Figure 4 device would operate with active and non-active chip select signals, as recited in claim 15. Indeed, as Patent Owner points out (PO Resp. 12), Petitioner's contentions for limitation 15.6 only rely on Halbert's Figure 2 prior art device. *See* Pet. 31–32. Petitioner's lack of explanation as to how active and non-active signals would affect the operation of Halbert's Figure 4 device is significant, as explained below.

Halbert's Figure 5 is reproduced below.



Halbert's Figure 5 is a timing diagram for two consecutive read operations for the memory module of Figure 4. Ex. 1005 ¶¶ 16, 37. Halbert explains that each of ranks 140 and 142 is "capable of performing m-bit-wide data transfers," and as shown in Halbert's Figure 4, reproduced above earlier in this section, bus RDQ0 corresponds to rank 140 and bus RDQ1 corresponds to rank 142. Ex. 1005 ¶ 30. With reference to Figure 5, Halbert explains that first and second read commands are clocked in at times T4 and T5, respectively. Ex. 1005 ¶ 37. "At T7n, device array 140/142 takes MDQS high, signifying that data outputs 'DO_a1' and 'DO_a2' are being driven respectively onto buses RDQ0 and RDQ1 at that time." Ex. 1005 ¶ 39. Halbert explains that at time T8n, "the memory devices begin data output of the results of the second READ operation," which is shown in Figure 5 as "DO_b1" on bus RDQ0 and "DO_b2" on bus RDQ1. Ex. 1005 ¶ 42.

Halbert discloses that multiplexer/demultiplexer (MUX/DeMUX) 124 in Figure 4 selects data from either register 126 or from register 128 to output to buffer 122, which are then output on line DQ. Ex. 1005 ¶ 33. Halbert explains that "[d]ata is serialized from the data registers onto the memory data bus by reading 2m bits into the data registers during one memory device read cycle, and then driving these bits, m at a time, through MUX 124." Ex. 1005 ¶ 33. As shown in Halbert's Figure 5, over one clock cycle (T7n–T8n), each of ranks 140 and 142 outputs one piece of m-bit-wide data, and over one clock cycle (T8–T9), those two pieces of m-bit-wide data are output on line DQ to the system memory data bus. Halbert explains that the second read operation proceeds in the same fashion as the first and that "[t]he net result is that the memory data bus transfers 4m bits of data in two memory bus clock cycles (four m-bit transfers), with only two data accesses performed at each memory device on the module." Ex. 1005 ¶ 42. Thus, Halbert's memory module outputs data to the system memory data bus at twice the rate that each of ranks 140 and 142 outputs data. *See* Ex. 2003 ¶¶ 68–73 (Dr. Przybylski's credible testimony explaining Halbert's data rates).

Dr. Przybylski testifies that Halbert operates "multiple memory ranks *concurrently* to increase bandwidth of the memory system." Ex. 2003 ¶ 119 (citing Ex. 1005 ¶¶ 24, 30; Ex. 2004, 84:19–85:9, 97:8–17). We credit this testimony because it is based on Halbert's express disclosure, as discussed above and shown in the Figure 5 timing diagram.

Turning back to the claim language, limitation 15.6 recites "the first plurality of registered chip select signals including a first registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value." Petitioner's

contentions correctly assert that Halbert's Figure 2 memory device would have active and non-active signals at the same time because one bank of memory devices would be selected while the other bank is not selected, as discussed above. *See* Pet. 31–32 (discussing Halbert's Figures 2 and 3). But these contentions do not address sufficiently the use of such signals in Halbert's Figure 4 memory module, which Petitioner contends is the recited "memory module" and which Petitioner proposes to modify with chip select signals. *See* Pet. 15–16 ("Halbert further discloses the components of a memory module, e.g., as depicted in Fig. 4 below."), 21–22 (asserting that it would have been obvious to include chip select signals in the Figure 4 memory module).

As discussed above, Halbert's Figure 5 shows ranks 140 and 142 operating concurrently to increase the throughput of the memory. This is not to say that Halbert cannot be configured to operate with active and non-active signals such that ranks 140 and 142 do not operate concurrently. Indeed, Halbert discloses that "*[g]enerally*, multiple ranks will receive the same address and commands, and will perform memory operations with the interface circuit concurrently" (Ex. 1005 ¶ 30 (emphasis added)), which suggests that the memory need not be limited to concurrently-operating ranks. But as the Federal Circuit has stated, "obviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention." *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1074 (Fed. Cir. 2015). Halbert's Figure 5 shows operating ranks 140 and 142 concurrently to increase memory throughput. If active and non-active signals are applied to ranks 140 and 142 in Halbert's Figure 5, the increased memory throughput would be eliminated by operating only one of the ranks at a time.

In other words, Halbert's Figure 4 memory module would operate at the rate of each of ranks 140 and 142, rather than "twice the data rate" of the ranks. *See* Ex. 1005 ¶ 24. Petitioner's analysis for limitation 15.6 does not sufficiently address Halbert's Figure 4, much less "explain why a person of ordinary skill in the art would have combined elements from specific references *in the way the claimed invention does*," accounting for the performance impact of not operating ranks 140 and 142 concurrently. *See ActiveVideo Networks, Inc. v. Verizon Comm'ns, Inc.*, 694 F.3d 1312, 1328 (Fed. Cir. 2012).

Therefore, Petitioner's contentions that using chip select signals would have been obvious in Halbert's Figure 4 do not sufficiently address the particular requirement of having a "first plurality of registered chip select signals including a first registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value."

Petitioner further argues that "it is undisputed that data from each rank in Fig. 4 is output onto the memory bus one rank at a time" and, therefore, that "a selection of which rank to output the data from must occur." Pet. Reply 5. Petitioner asserts that bodily incorporation is not the test for obviousness but that "the prior art registered chip select signals operation concepts described with respect to Figs. 2 and 3 could have been implemented in Fig. 4 in a variety of well-known and obvious ways." Pet. Reply 6–7. According to Petitioner,

> the use of active and non-active chip select signals (similar in operation to RDQS and REG#_SEL) could be used to trigger selecting DO_a1 from rank 140 (and not DO_a2 from rank 142) to be sent to buffer 122, while active and non-active chip select

> signals for ranks 142 and 140, respectively, are used a half-clock cycle later to send DO_a2 onto the memory bus.

Pet. Reply 7 (citing *Uber Techs., Inc. v. X One, Inc.*, 957 F.3d 1334, 1341 (Fed. Cir. 2020)).

These arguments are not persuasive. We agree with Petitioner that there is ultimately a selection of data between ranks 140 and 142 to put onto the memory bus during a read operation. Halbert explains that this is performed by multiplexer/demultiplexer (MUX/DeMUX) 124 as follows: "either data signals DQ0 (from register 126) or data signals DQ1 (from register 128) can be multiplexed to buffer 122 when the module is reading from memory device array 140/142." Ex. 1005 ¶ 33. This selection happens using signals DIR and REG_SEL after registers 126 and 128 have received data from ranks 140 and 142 in a read operation. Ex. 1005 ¶¶ 32–35.

But Petitioner's argument falls short if the chip select signals are only used for selecting at the MUX/DeMUX because claims 15 and 28 recite that the memory devices are "configured to receive respective ones of the plurality of registered chip select signals." If the active and non-active signals are only used at the MUX/DeMUX and are not sent to the memory devices (ranks 140 and 142), then the combination does not show memories that are "configured to receive respective ones of the plurality of registered chip select signals." Thus, we find Petitioner's reliance on *Uber Technologies* misplaced because Petitioner's Reply contentions do not show a "predictable variation" of Halbert's Figure 4 that still meets the claims. *See Uber Techs.*, 957 F.3d at 1340 ("The combination of Okubo with Konishi's known server-side plotting is obvious because it would have been a 'predictable variation' of Okubo's system as written, using a technique that

was known to one of ordinary skill in the art." (quoting *KSR*, 550 U.S. at 417)).

Furthermore, Petitioner's argument that bodily incorporation is not the test for obviousness is misplaced because the combined teachings do not suggest the subject matter of recitation 15.6. That is, Petitioner has not provided adequate reasoning to apply active and non-active chip select signals to ranks 140 and 142, as discussed above.

For all the reasons discussed above, Petitioner has not proven by a preponderance of the evidence that the subject matter of claims 15 and 28 would have been obvious over the combined teachings of Halbert and JESD21-C. Dependent claims 16–20, 22–27, and 29–33 stand with their respective independent claims.

III. CONCLUSION

For the reasons discussed above, we determine that Petitioner has not proven, by a preponderance of the evidence, that claims 15–20 and 22–33 of the '314 patent are unpatentable, as summarized in the following table:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
15–20, 22–33	103(a)	Halbert, JESD21-C		15–20, 22–33

IV. ORDER

Accordingly, it is

ORDERED that claims 15–20 and 22–33 of the '314 patent have not been shown to be unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2022-00744
Patent 10,489,314 B2

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(12) **United States Patent**
Solomon et al.

(10) **Patent No.: US 10,489,314 B2**
(45) **Date of Patent: Nov. 26, 2019**

(54) **MEMORY MODULE WITH DATA BUFFERING**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **15/857,519**

(22) Filed: **Dec. 28, 2017**

(65) **Prior Publication Data**

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Related U.S. Application Data

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(51) **Int. Cl.**
G06F 12/00 (2006.01)
G06F 13/16 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***G06F 13/1673*** (2013.01); ***G06F 12/00*** (2013.01); ***G06F 13/00*** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC G06F 13/1673; G06F 12/00; G06F 13/00; G06F 13/4243; G06F 13/4282
See application file for complete search history.

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Primary Examiner — Gurtej Bansal
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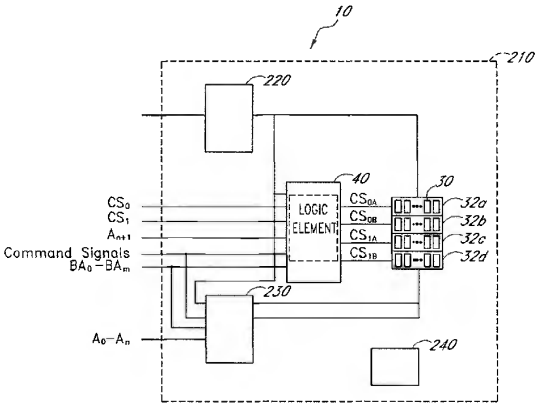
(57) **ABSTRACT**

A memory module operable to communicate data with a memory controller via a data bus comprises a plurality of memory integrated circuits including first memory integrated circuits and second memory integrated circuits, a data buffer coupled between the first memory integrated circuits and the data bus, and between the second memory integrated circuits and the data bus, and logic coupled to the data buffer. The logic is configured to respond to a first memory command by providing first control signals to the data buffer to enable communication of at least one first data signal between the first memory integrated circuits and the memory controller through the data buffer, and is further configured to respond to a second memory command by providing second control signals to the data buffer to enable communication of at least one second data signal between the second memory integrated circuit and the memory controller through the data buffer.

33 Claims, 23 Drawing Sheets



Related U.S. Application Data

continuation of application No. 13/971,231, filed on Aug. 20, 2013, now Pat. No. 9,037,774, which is a continuation of application No. 13/287,081, filed on Nov. 1, 2011, now Pat. No. 8,516,188, which is a continuation of application No. 13/032,470, filed on Feb. 22, 2011, now Pat. No. 8,081,536, which is a continuation of application No. 12/955,711, filed on Nov. 29, 2010, now Pat. No. 7,916,574, which is a continuation of application No. 12/629,827, filed on Dec. 2, 2009, now Pat. No. 7,881,150, which is a continuation of application No. 12/408,652, filed on Mar. 20, 2009, now Pat. No. 7,636,274, which is a continuation of application No. 11/335,875, filed on Jan. 19, 2006, now Pat. No. 7,532,537, which is a continuation-in-part of application No. 11/173,175, filed on Jul. 1, 2005, now Pat. No. 7,289,386, which is a continuation-in-part of application No. 11/075,395, filed on Mar. 7, 2005, now Pat. No. 7,286,436.

(60) Provisional application No. 60/645,087, filed on Jan. 19, 2005, provisional application No. 60/588,244, filed on Jul. 15, 2004, provisional application No. 60/550,668, filed on Mar. 5, 2004, provisional application No. 60/575,595, filed on May 28, 2004, provisional application No. 60/590,038, filed on Jul. 21, 2004.

(51) **Int. Cl.**

G11C 5/04	(2006.01)
G06F 13/00	(2006.01)
G06F 13/42	(2006.01)
G11C 7/10	(2006.01)
G11C 15/00	(2006.01)

(52) **U.S. Cl.**

CPC ***G06F 13/4243*** (2013.01); ***G06F 13/4282*** (2013.01); ***G11C 5/04*** (2013.01); ***G11C 7/1072*** (2013.01); ***G11C 15/00*** (2013.01)

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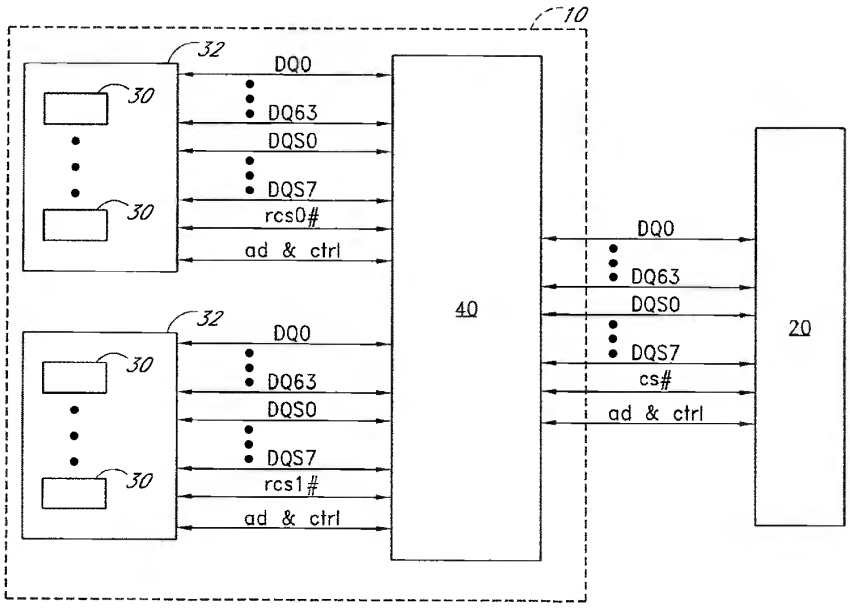
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FIG. 1

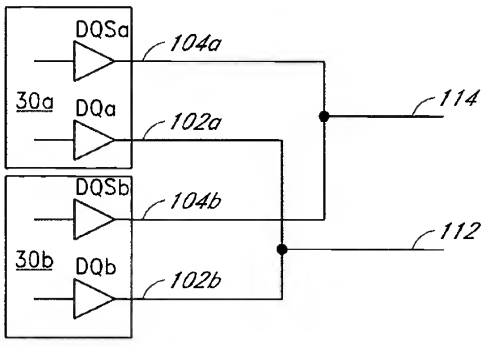

FIG. 2

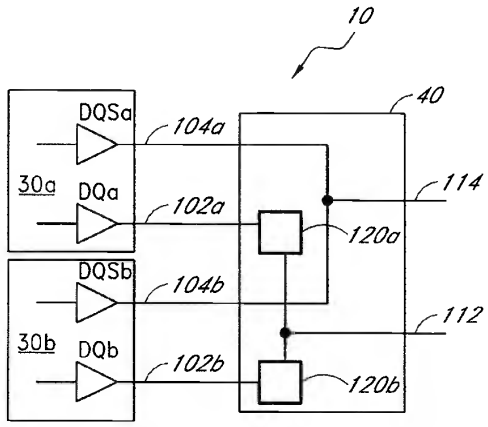
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FIG. 3A

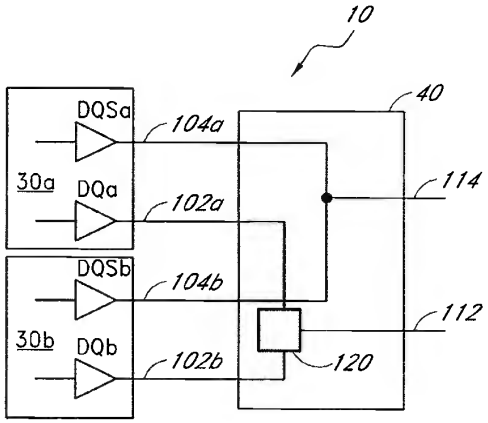
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FIG. 3B

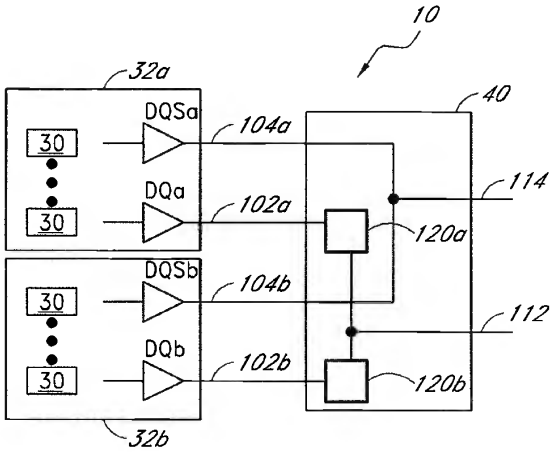
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FIG. 4A

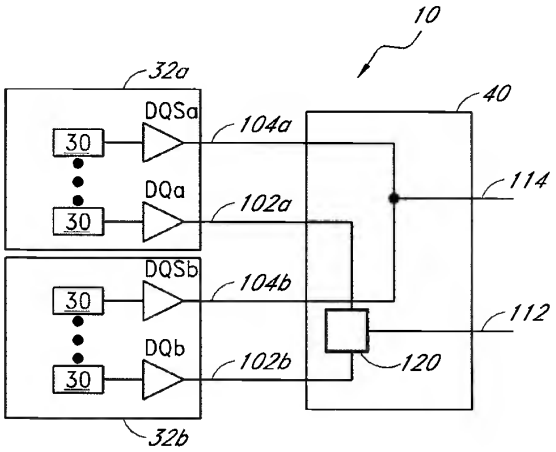
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FIG. 4B

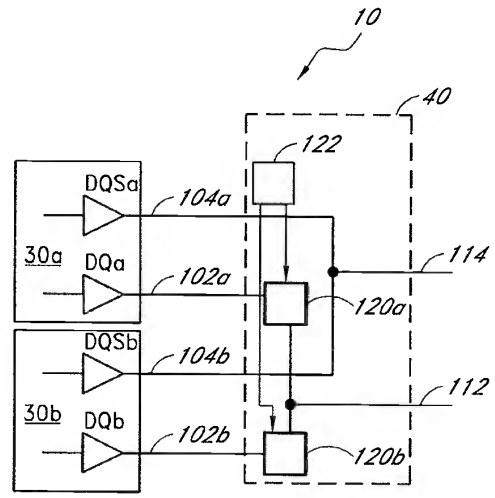
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FIG. 5A

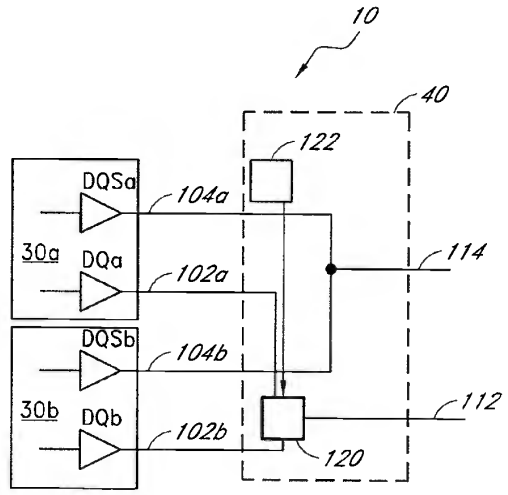
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FIG. 5B

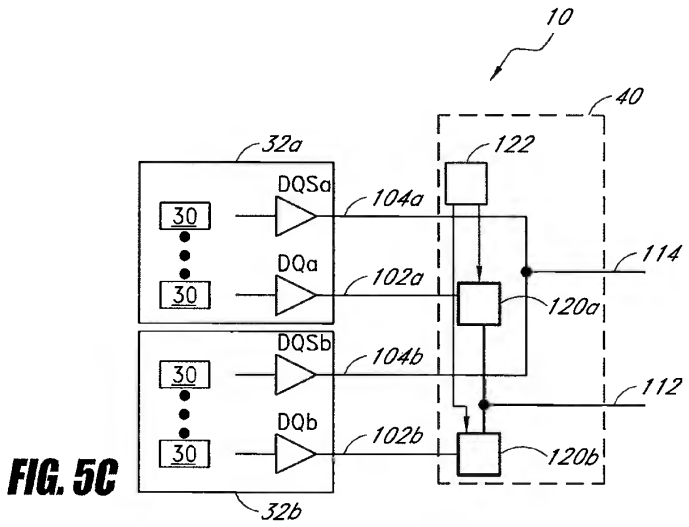
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FIG. 5C

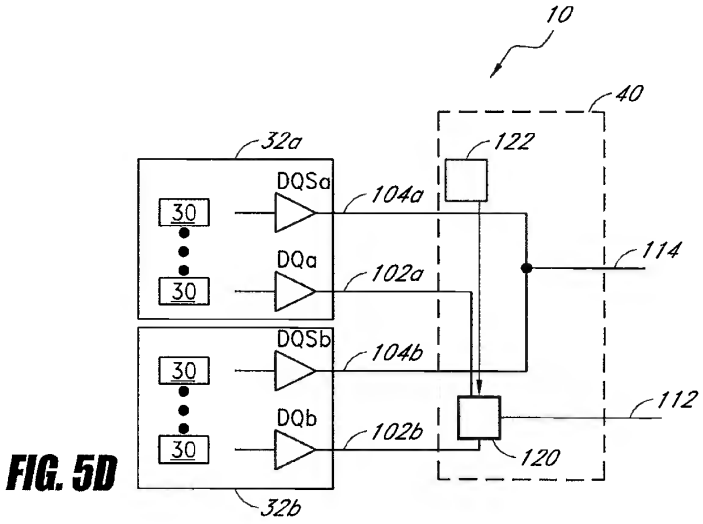
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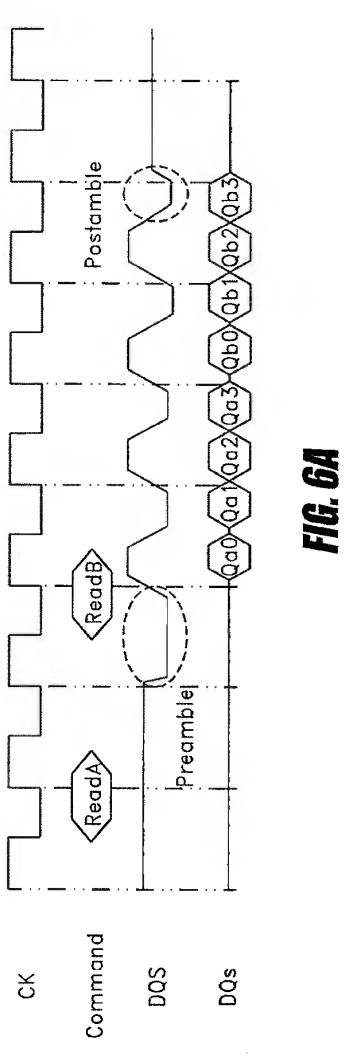
FIG. 5D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Qb3

FIG. 6A

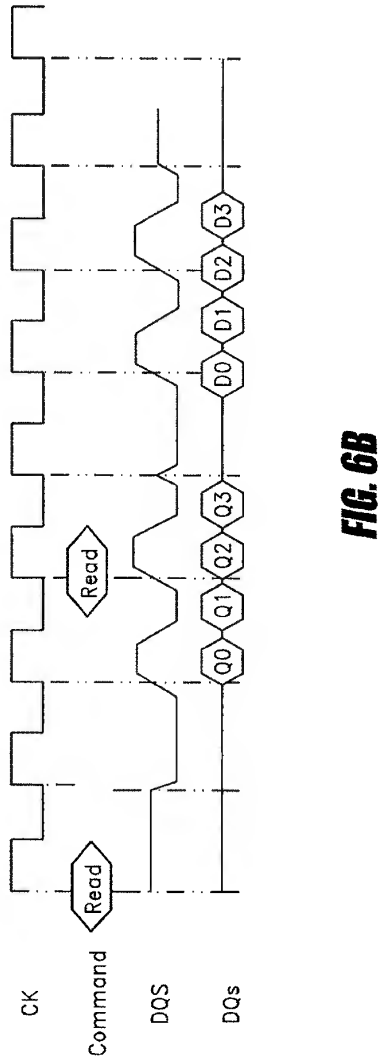
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FIG. 6B

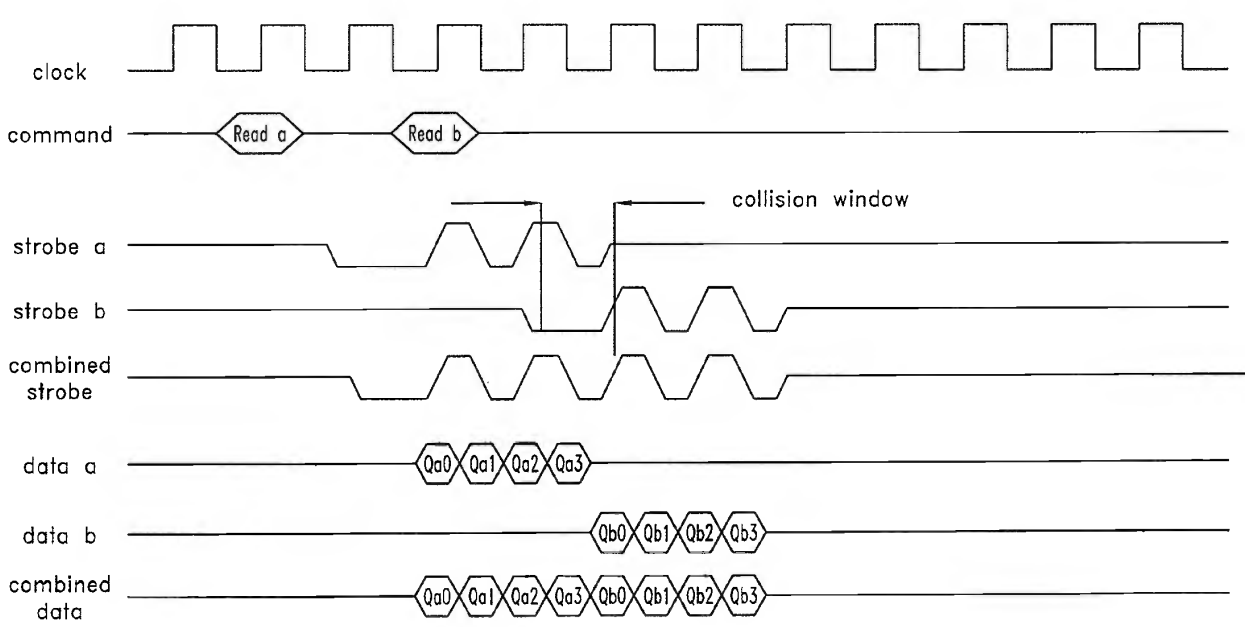

FIG. 7

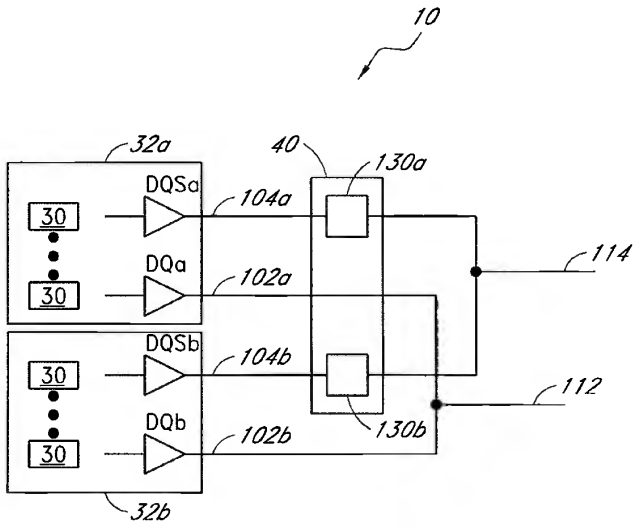
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FIG. 8A

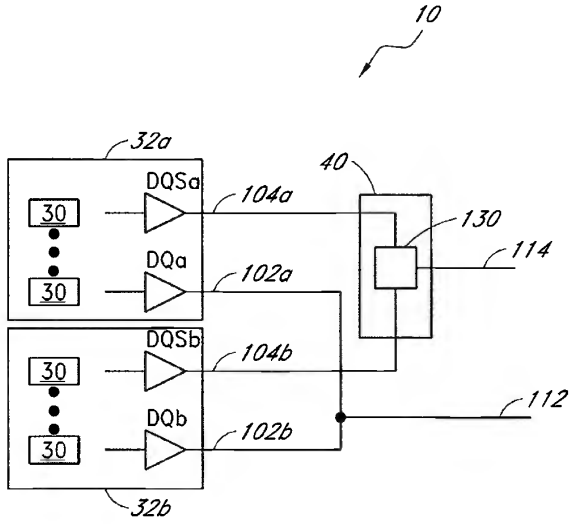
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FIG. 8B

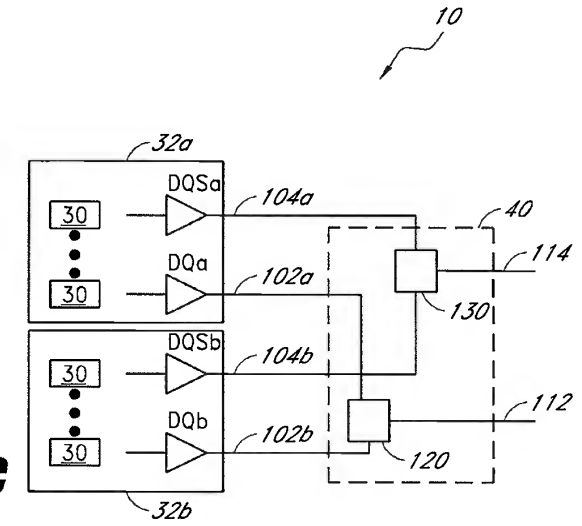
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FIG. 8C

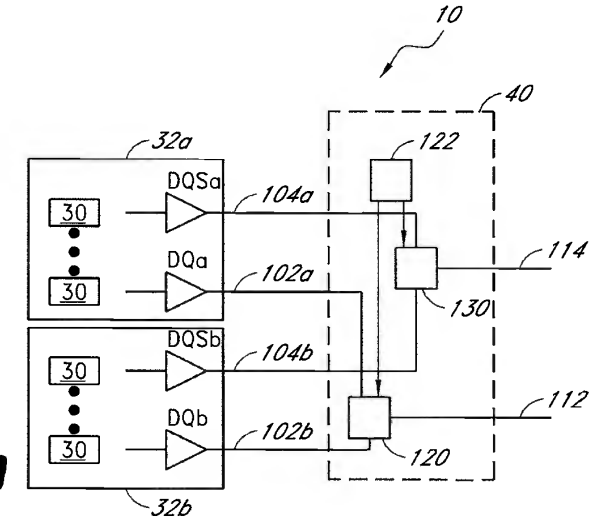
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FIG. 8D

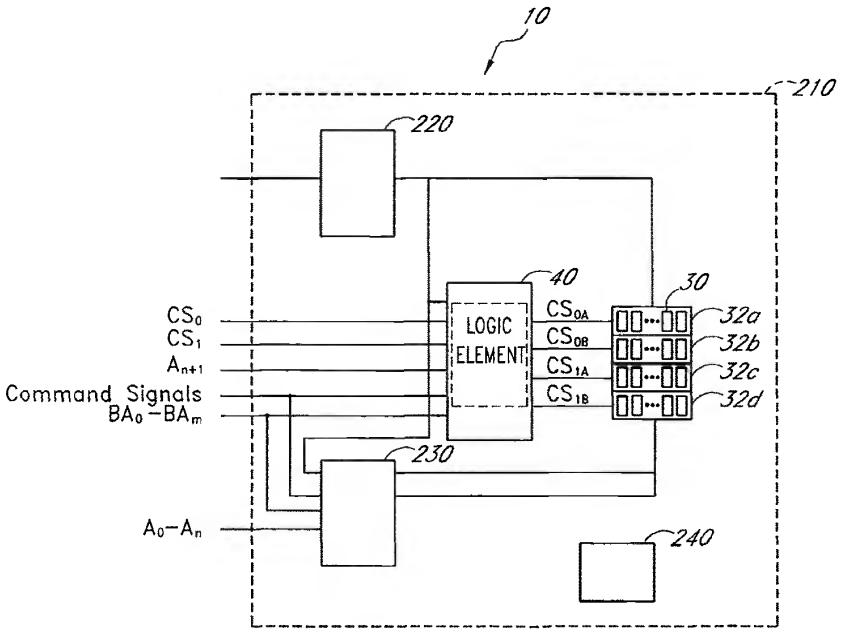
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FIG. 9A

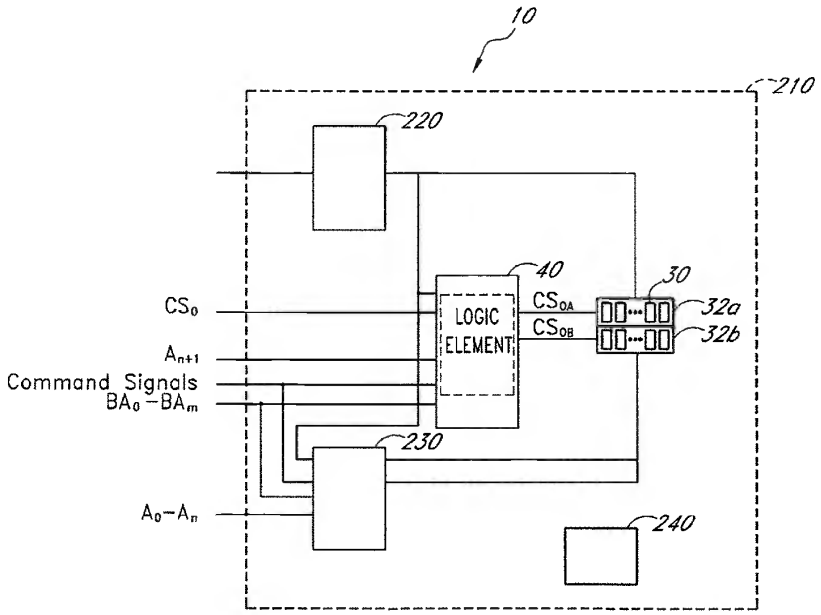
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FIG. 9B

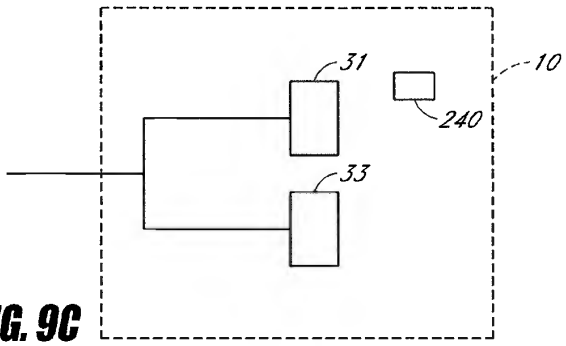

FIG. 9C

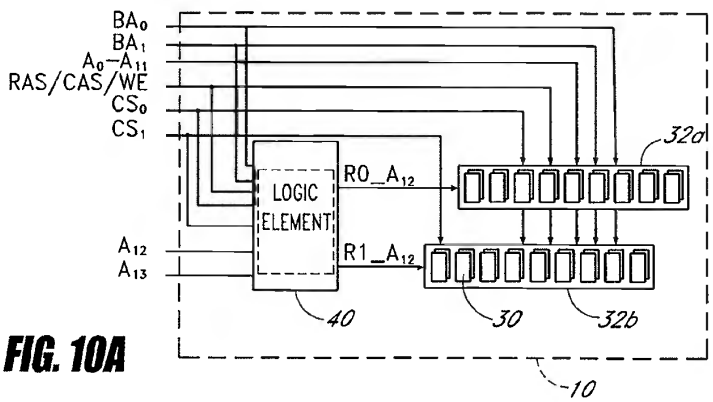

FIG. 10A

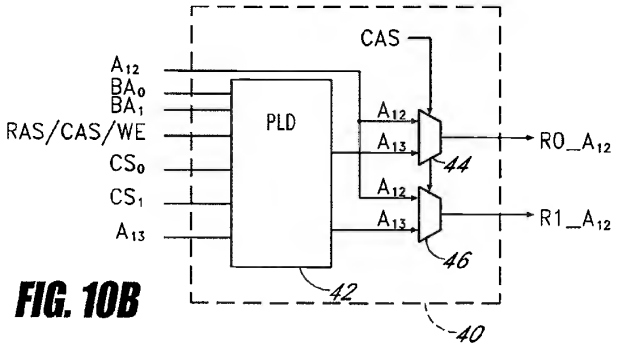

FIG. 10B

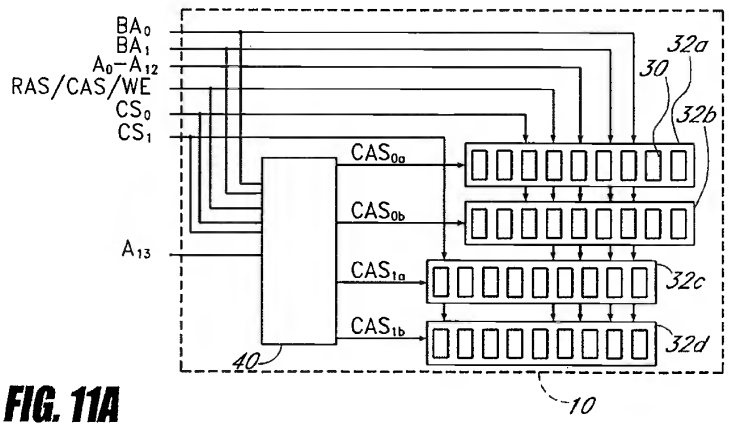

FIG. 11A

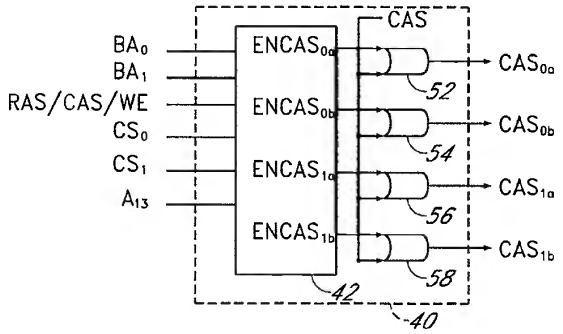

FIG. 11B

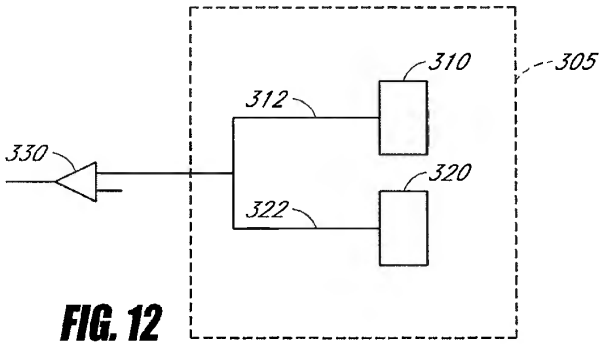

FIG. 12

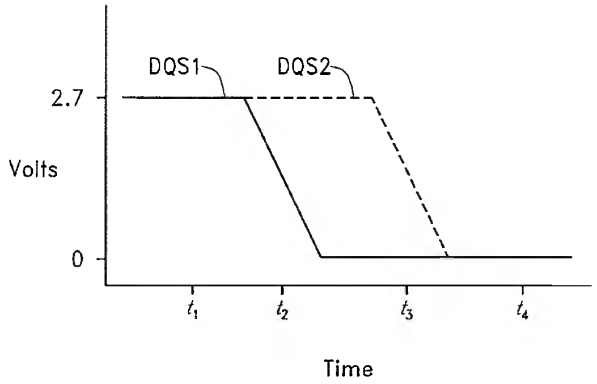

FIG. 13

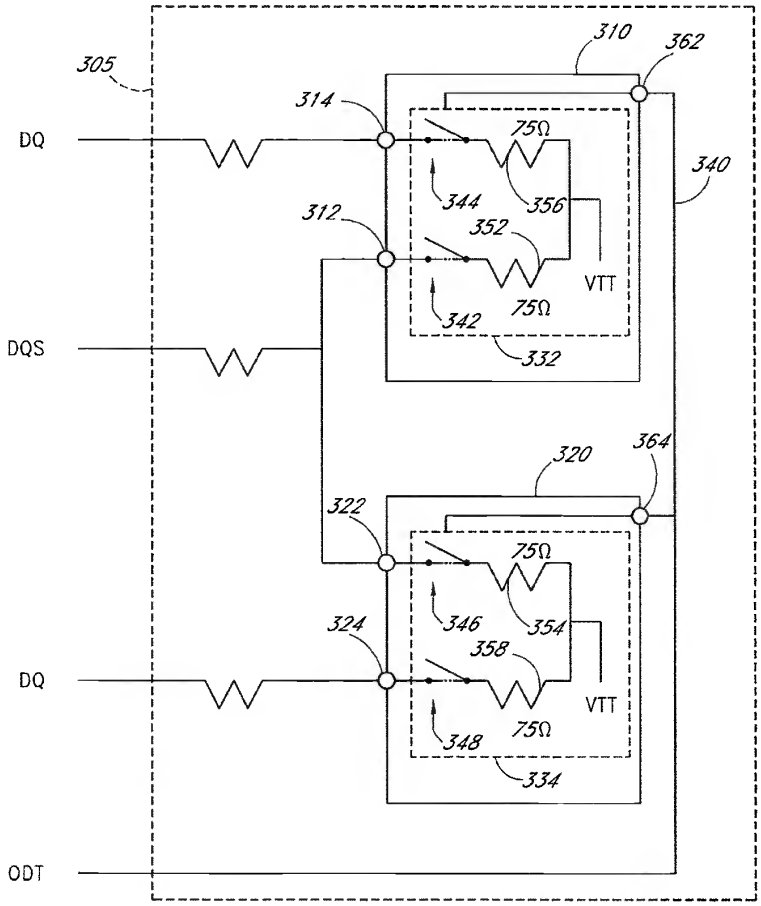
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FIG. 14

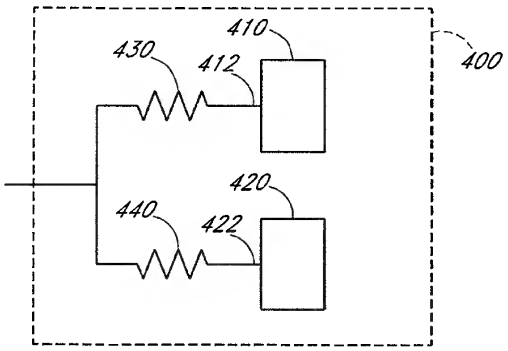

FIG. 15

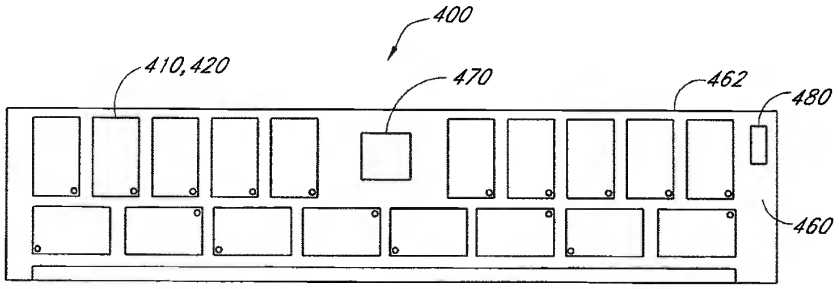

FIG. 16A

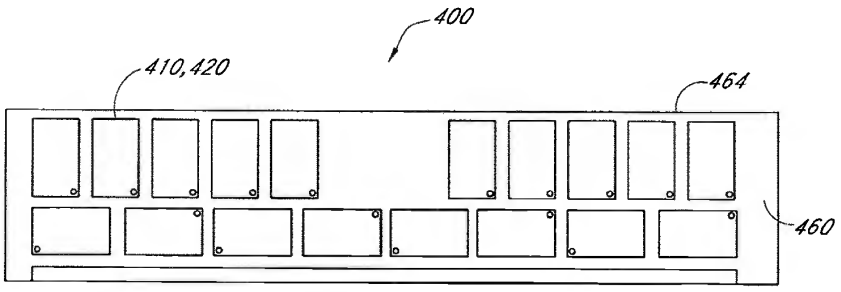

FIG. 16B

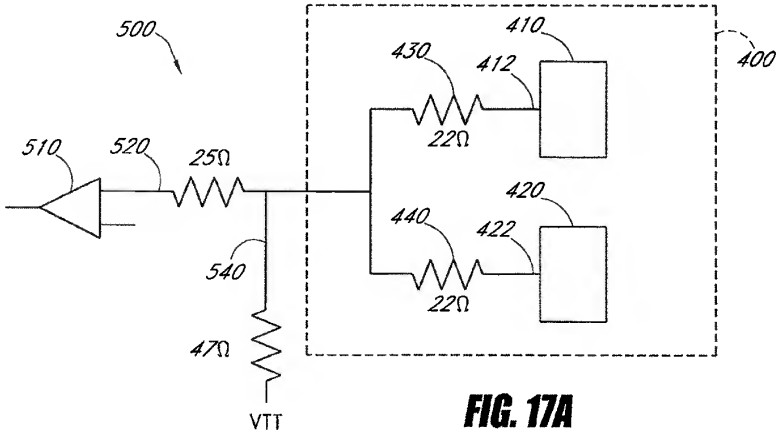

FIG. 17A

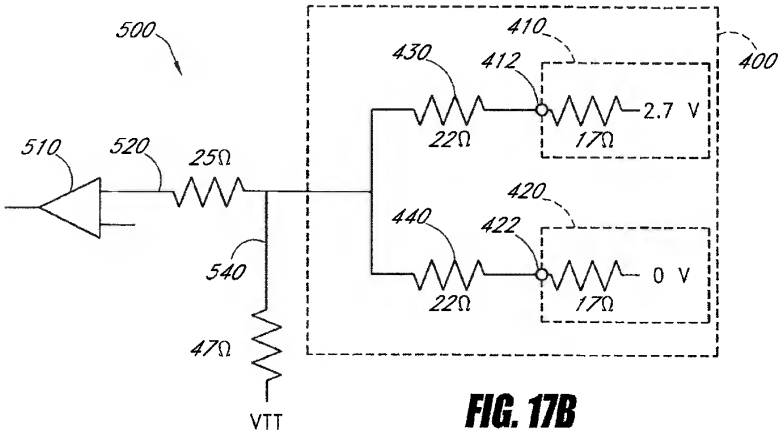

FIG. 17B

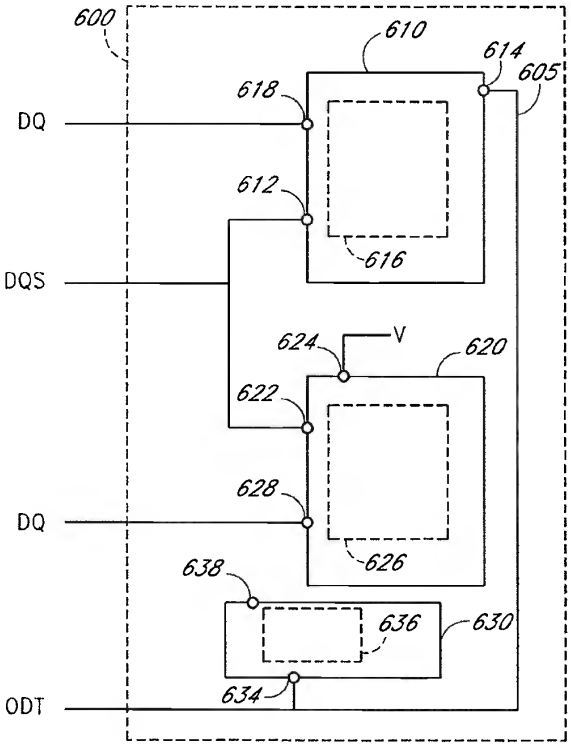
600
610
614
605
618
DQ
612
616
DQS
624
V
620
622
628
DQ
626
638
636
630
634
ODT

FIG. 18

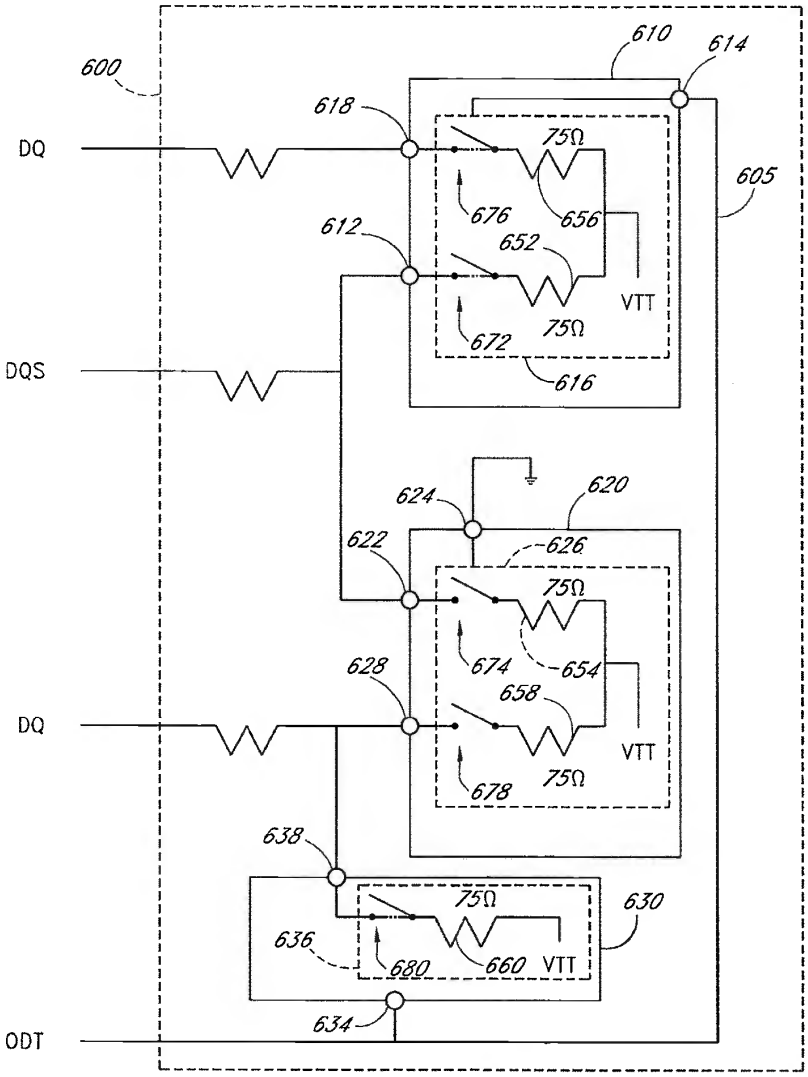
600
610
614
618
DQ
75Ω
605
676
656
612
652
VTT
672
75Ω
DQS
616
624
620
622
626
75Ω
674
654
628
658
DQ
VTT
678
75Ω
638
75Ω
630
636
680
660
VTT
634
ODT

FIG. 19

MEMORY MODULE WITH DATA BUFFERING

CROSS-REFERENCE TO RELATED APPLICATIONS

The present application is a continuation of U.S. patent application Ser. No. 14/715,486, filed May 18, 2015, to be issued as U.S. Pat. No. 9,858,215 on Jan. 2, 2018, which is a continuation of U.S. patent application Ser. No. 13/971,231, filed Aug. 20, 2013, now U.S. Pat. No. 9,037,774, which is a continuation of U.S. patent application Ser. No. 13/287,081, filed Nov. 1, 2011, now U.S. Pat. No. 8,516,188, which is a continuation of U.S. patent application Ser. No. 13/032,470, filed Feb. 22, 2011, now U.S. Pat. No. 8,081,536, which is a continuation of U.S. patent application Ser. No. 12/955,711, filed Nov. 29, 2010, now U.S. Pat. No. 7,916,574, which is a continuation of U.S. patent application Ser. No. 12/629,827, filed Dec. 2, 2009, now U.S. Pat. No. 7,881,150. which is a continuation of U.S. patent application Ser. No. 12/408,652, filed Mar. 20, 2009, now U.S. Pat. No. 7,636,274, which is a continuation of U.S. patent application Ser. No. 11/335,875, filed Jan. 19, 2006, now U.S. Pat. No. 7,532,537, which claims the benefit of U.S. Provisional Appl. No. 60/645,087, filed Jan. 19, 2005 and which is a continuation-in-part of U.S. patent application Ser. No. 11/173,175, filed Jul. 1, 2005, now U.S. Pat. No. 7,289,386, which claims the benefit of U.S. Provisional Appl. No. 60/588,244, filed Jul. 15, 2004 and which is a continuation-in-part of U.S. patent application Ser. No. 11/075,395, filed Mar. 7, 2005, now U.S. Pat. No. 7,286,436, which claims the benefit of U.S. Provisional Appl. No. 60/550,668, filed Mar. 5, 2004, U.S. Provisional Appl. No. 60/575,595, filed May 28, 2004, and U.S. Provisional Appl. No. 60/590,038, filed Jul. 21, 2004, U.S. patent application Ser. Nos. 13/287,081, 13/032,470, 12/955,711, 12/629,827, 12/408,652, 11/335,875, 11/173,175, and 11/075,395, and U.S. Provisional Appl. Nos. 60/550,668, 60/575,595, 60/590,038, 60/588,244, and 60/645,087 are each incorporated in its entirety by reference herein.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to memory modules of a computer system, and more specifically to devices and methods for improving the performance, the memory capacity, or both, of memory modules.

2. Description of the Related Art

Certain types of memory modules comprise a plurality of dynamic random-access memory (DRAM) devices mounted on a printed circuit board (PCB). These memory modules are typically mounted in a memory slot or socket of a computer system (e.g., a server system or a personal computer) and are accessed by the processor of the computer system. Memory modules typically have a memory configuration with a unique combination of rows, columns, and banks which result in a total memory capacity for the memory module.

For example, a 512-Megabyte memory module (termed a "512-MB" memory module, which actually has 2^{29} or 536,870,912 bytes of capacity) will typically utilize eight 512-Megabit DRAM devices (each identified as a "512-Mb" DRAM device, each actually having 2^{29} or 536,870,912 bits of capacity). The memory cells (or memory locations) of each 512-Mb DRAM device can be arranged in four banks, with each bank having an array of 2^{24} (or 16,777,216) memory locations arranged as 2^{13} rows and 2^{11} columns, and with each memory location having a width of 8 bits. Such DRAM devices with 64 M 8-bit-wide memory locations (actually with four banks of 2^{27} or 134,217,728 one-bit memory cells arranged to provide a total of 2^{26} or 67,108,864 memory locations with 8 bits each) are identified as having a "64 Mb×8" or "64 M×8-bit" configuration, or as having a depth of 64 M and a bit width of 8. Furthermore, certain commercially-available 512-MB memory modules are termed to have a "64 M×8-byte" configuration or a "64 M×64-bit" configuration with a depth of 64 M and a width of 8 bytes or 64 bits.

Similarly, a 1-Gigabyte memory module (termed a "1-GB" memory module, which actually has 2^{30} or 1,073,741,824 bytes of capacity) can utilize eight 1-Gigabit DRAM devices (each identified as a "1-Gb" DRAM device, each actually having 2^{30} or 1,073,741,824 bits of capacity). The memory locations of each 1-Gb DRAM device can be arranged in four banks, with each bank having an array of memory locations with 2^{14} rows and 2^{11} columns, and with each memory location having a width of 8 bits. Such DRAM devices with 128 M 8-bit-wide memory locations (actually with a total of 2^{27} or 134,217,728 memory locations with 8 bits each) are identified as having a "128 Mb×8" or "128 M×8-bit" configuration, or as having a depth of 128 M and a bit width of 8. Furthermore, certain commercially-available 1-GB memory modules are identified as having a "128 M×8-byte" configuration or a "128 M×64-bit" configuration with a depth of 128 M and a width of 8 bytes or 64 bits.

The commercially-available 512-MB (64 M×8-byte) memory modules and the 1-GB (128 M×8-byte) memory modules described above are typically used in computer systems (e.g., personal computers) which perform graphics applications since such "×8" configurations are compatible with data mask capabilities often used in such graphics applications. Conversely, memory modules with "×4" configurations are typically used in computer systems such as servers which are not as graphics-intensive. Examples of such commercially available "×4" memory modules include, but are not limited to, 512-MB (128 M×4-byte) memory modules comprising eight 512-Mb (128 Mb×4) memory devices.

The DRAM devices of a memory module are generally arranged as ranks or rows of memory, each rank of memory generally having a bit width. For example, a memory module in which each rank of the memory module is 64 bits wide is described as having an "×64" organization. Similarly, a memory module having 72-bit-wide ranks is described as having an "×72" organization.

The memory capacity of a memory module increases with the number of memory devices. The number of memory devices of a memory module can be increased by increasing the number of memory devices per rank or by increasing the number of ranks. For example, a memory module with four ranks has double the memory capacity of a memory module with two ranks and four times the memory capacity of a memory module with one rank. Rather than referring to the memory capacity of the memory module, in certain circumstances, the memory density of the memory module is referred to instead.

During operation, the ranks of a memory module are selected or activated by address and command signals that are received from the processor. Examples of such address and command signals include, but are not limited to, rank-

select signals, also called chip-select signals. Most computer and server systems support one-rank and two-rank memory modules. By only supporting one-rank and two-rank memory modules, the memory density that can be incorporated in each memory slot is limited.

Various aspects of the design of a memory module impose limitations on the size of the memory arrays of the memory module. Certain such aspects are particularly important for memory modules designed to operate at higher frequencies. Examples of such aspects include, but are not limited to, memory device (e.g., chip) densities, load fan-out, signal integrity, available rank selects, power dissipation, and thermal profiles.

SUMMARY OF THE INVENTION

In certain embodiments, a memory module is operable to communicate data with a memory controller via a data bus in response to memory commands received from the memory controller. The memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst. The memory module comprises a plurality of memory integrated circuits including at least one first memory integrated circuit and at least one second memory integrated circuit, and further comprises a buffer coupled between the at least one first memory integrated circuit and the data bus, and between the at least one second memory integrated circuit and the data bus. The buffer couples the at least one first memory integrated circuit to the data bus and isolates the at least one second memory integrated circuit from the data bus while the memory module is receiving or outputting the first data burst in response to the first memory command. The buffer then couples the at least one second memory integrated circuit to the data bus and isolates the at least one first memory integrated circuit from the data bus while the memory module is receiving or outputting the second data burst in response to the second memory command.

Certain embodiments provide a method of operating a memory module coupled to a memory controller via a memory bus that includes a control/address (C/A) bus and a data bus. The memory module comprises memory integrated circuits, including at least one first memory integrated circuit and at least one second memory integrated circuit. The method comprises receiving from the memory controller a first set of input C/A signals associated with a first memory command via the C/A bus, the first memory command to cause the memory module to receive or output a first data burst; generating a first set of output C/A signals in response to the first set of input C/A signals, the first set of output C/A signals causing the at least one first memory integrated circuit to receive or output the first data burst; receiving from the memory controller a second set of input control/address signals associated with a second memory command via the C/A bus, the second memory command to cause the memory module to receive or output a second data burst: generating a second set of output C/A signals in response to the second set of input C/A signals, the second set of output C/A signals causing the at least one second memory integrated circuit to receive or output the second data burst; coupling the at least one first memory integrated circuit to the data bus and isolating the at least one second memory integrated circuit from the data bus while the memory module is receiving or outputting the first data burst in response to the first memory command; and coupling the at least one second memory integrated circuit to the data bus and isolating the at least one first memory integrated circuit from the data bus while the memory module is receiving or outputting the second data burst in response to the second memory command.

In certain embodiments, a circuit is configured to be mounted on a memory module that is operable to communicate data with a memory controller via a data bus in response to memory commands received from the memory controller. The memory module including at least one first memory integrated circuit and at least one second memory integrated circuit. The memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the at least one first memory integrated circuit to receive or output a first data burst and the second memory command to cause the at least one second memory integrated circuit to receive or output a second data burst. The circuit comprises logic that couples the at least one first memory integrated circuit to the data bus and that isolates the at least one second memory integrated circuit from the data bus while the memory module is receiving or outputting the first data burst in response to the first memory command. The logic then couples the at least one second memory integrated circuit to the data bus and isolates the at least one first memory integrated circuit from the data bus while the memory module is receiving or outputting the second data burst in response to the second memory command

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** schematically illustrates an example memory module in accordance with certain embodiments described herein.

FIG. **2** schematically illustrates a circuit diagram of two memory devices of a conventional memory module.

FIGS. **3**A and **3**B schematically illustrate example memory modules having a circuit which selectively isolates one or both of the DQ data signal lines of the two memory devices from the computer system in accordance with certain embodiments described herein.

FIGS. **4**A and **4**B schematically illustrate example memory modules having a circuit which selectively isolates one or both of the DQ data signal lines of the two ranks of memory devices from the computer system in accordance with certain embodiments described herein.

FIGS. **5**A-**5**D schematically illustrate example memory modules having a circuit comprising a logic element and one or more switches operatively coupled to the logic element in accordance with certain embodiments described herein.

FIG. **6**A shows an exemplary timing diagram of a gapless read burst for a back-to-back adjacent read condition from one memory device.

FIG. **6**B shows an exemplary timing diagram with an extra clock cycle between successive read commands issued to different memory devices for successive read accesses from different memory devices.

FIG. **7** shows an exemplary timing diagram in which the last data strobe of memory device "a" collides with the pre-amble time interval of the data strobe of memory device "b."

FIGS. **8**A-**8**D schematically illustrate circuit diagrams of example memory modules comprising a circuit which multiplexes the DQS data strobe signal lines from one another in accordance with certain embodiments described herein.

FIG. **9**A schematically illustrates an example memory module with four ranks of memory devices compatible with certain embodiments described herein.

FIG. **9**B schematically illustrates an example memory module with two ranks of memory devices compatible with certain embodiments described herein.

FIG. **9**C schematically illustrates another example memory module in accordance with certain embodiments described herein.

FIG. **10**A schematically illustrates an exemplary memory module which doubles the rank density in accordance with certain embodiments described herein.

FIG. **10**B schematically illustrates an exemplary circuit compatible with embodiments described herein.

FIG. **11**A schematically illustrates an exemplary memory module which doubles number of ranks in accordance with certain embodiments described herein.

FIG. **11**B schematically illustrates an exemplary circuit compatible with embodiments described herein.

FIG. **12** schematically illustrates an exemplary memory module in which a data strobe (DQS) pin of a first memory device is electrically connected to a DQS pin of a second memory device while both DQS pins are active.

FIG. **13** is an exemplary timing diagram of the voltages applied to the two DQS pins due to non-simultaneous switching.

FIG. **14** schematically illustrates another exemplary memory module in which a DQS pin of a first memory device is connected to a DQS pin of a second memory device.

FIG. **15** schematically illustrates an exemplary memory module in accordance with certain embodiments described herein.

FIGS. **16**A and **16**B schematically illustrate a first side and a second side, respectively, of a memory module with eighteen 64 M×4 bit, DDR-1 SDRAM FBGA memory devices on each side of a 184-pin glass-epoxy printed circuit board.

FIGS. **17**A and **17**B schematically illustrate an exemplary embodiment of a memory module in which a first resistor and a second resistor are used to reduce the current flow between the first DQS pin and the second DQS pin.

FIG. **18** schematically illustrates another exemplary memory module compatible with certain embodiments described herein.

FIG. **19** schematically illustrates a particular embodiment of the memory module schematically illustrated by FIG. **18**.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

Load Isolation

FIG. **1** schematically illustrates an example memory module **10** compatible with certain embodiments described herein. The memory module **10** is connectable to a memory controller **20** of a computer system (not shown). The memory module **10** comprises a plurality of memory devices **30**, each memory device **30** having a corresponding load. The memory module **10** further comprises a circuit **40** electrically coupled to the plurality of memory devices **30** and configured to be electrically coupled to the memory controller **20** of the computer system. The circuit **40** selectively isolates one or more of the loads of the memory devices from the computer system. The circuit **40** comprises logic which translates between a system memory domain of the computer system and a physical memory domain of the memory module **10**.

As used herein, the term "load" is a broad term which includes, without limitation, electrical load, such as capacitive load, inductive load, or impedance load. As used herein, the term "isolation" is a broad term which includes, without limitation, electrical separation of one or more components from another component or from one another. As used herein, the term "circuit" is a broad term which includes, without limitation, an electrical component or device, or a configuration of electrical components or devices which are electrically or electromagnetically coupled together (e.g., integrated circuits), to perform specific functions.

Various types of memory modules **10** are compatible with embodiments described herein. For example, memory modules **10** having memory capacities of 512-MB, 1-GB, 2-GB, 4-GB, 8-GB, as well as other capacities, are compatible with embodiments described herein. Certain embodiments described herein are applicable to various frequencies including, but not limited to 100 MHz, 200 MHz, 400 MHz, 800 MHz, and above. In addition, memory modules **10** having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein. In certain embodiments, the memory module **10** comprises a printed circuit board on which the memory devices **30** are mounted, a plurality of edge connectors configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system, and a plurality of electrical conduits which electrically couple the memory devices **30** to the circuit **40** and which electrically couple the circuit **40** to the edge connectors. Furthermore, memory modules **10** compatible with embodiments described herein include, but are not limited to, single in-line memory modules (SIMMs), dual in-line memory modules (DIMMs), small-outline DIMMs (SO-DIMMs), unbuffered DIMMs (UDIMMs), registered DIMMs (RDIMMs), fully-buffered DIMM (FB-DIMM), rank-buffered DIMMs (RBDIMMs), mini-DIMMs, and micro-DIMMs.

Memory devices **30** compatible with embodiments described herein include, but are not limited to, random-access memory (RAM), dynamic random-access memory (DRAM), synchronous DRAM (SDRAM), and double-data-rate DRAM (e.g., SDR, DDR-1, DDR-2, DDR-3). In addition, memory devices **30** having bit widths of **4**, 8, 16, 32, as well as other bit widths, are compatible with embodiments described herein. Memory devices **30** compatible with embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP). ball-grid-array (BGA), fine-pitch BGA (FBGA), micro-BGA (μBGA), mini-BGA (mBGA), and chip-scale packaging (CSP). Memory devices **30** compatible with embodiments described herein are available from a number of sources, including but not limited to, Samsung Semiconductor, Inc. of San Jose, Calif., Infineon Technologies AG of San Jose, Calif., and Micron Technology, Inc. of Boise, Id. Persons skilled in the art can select appropriate memory devices **30** in accordance with certain embodiments described herein.

In certain embodiments, the plurality of memory devices **30** comprises a first number of memory devices **30**. In certain such embodiments, the circuit **40** selectively isolates a second number of the memory devices **30** from the computer system, with the second number less than the first number.

In certain embodiments, the plurality of memory devices **30** are arranged in a first number of ranks. For example, in certain embodiments, the memory devices **30** are arranged in

two ranks, as schematically illustrated by FIG. **1**. In other embodiments, the memory devices **30** are arranged in four ranks. Other numbers of ranks of the memory devices **30** are also compatible with embodiments described herein.

In certain embodiments, the circuit comprises a logic element selected from a group consisting of: a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA), a custom-designed semiconductor device, and a complex programmable-logic device (CPLD). In certain embodiments, the logic element of the circuit **40** is a custom device. Sources of logic elements compatible with embodiments described herein include, but are not limited to, Lattice Semiconductor Corporation of Hillsboro, Oreg., Altera Corporation of San Jose, Calif., and Xilinx Incorporated of San Jose, Calif. In certain embodiments, the logic element comprises various discrete electrical elements, while in certain other embodiments, the logic element comprises one or more integrated circuits.

In certain embodiments, the circuit **40** further comprises one or more switches which are operatively coupled to the logic element to receive control signals from the logic element. Examples of switches compatible with certain embodiments described herein include, but are not limited to, field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Tex.

FIG. **2** schematically illustrates a circuit diagram of two memory devices **30***a*, **30***b* of a conventional memory module showing the interconnections between the DQ data signal lines **102***a*, **102***b* of the memory devices **30***a*, **30***b* and the DQS data strobe signal lines **104***a*, **104***b* of the memory devices **30***a*, **30***b*. Each of the memory devices **30***a*, **30***b* has a plurality of DQ data signal lines and a plurality of DQS data strobe signal lines, however, for simplicity, FIG. **2** only illustrates a single DQ data signal line and a single DQS data strobe signal line for each memory device **30***a*, **30***b*. The DQ data signal lines **102***a*, **102***b* and the DQS data strobe signal lines **104***a*, **104***b* are typically conductive traces etched on the printed circuit board of the memory module. As shown in FIG. **2**, each of the memory devices **30***a*, **30***b* has their DQ data signal lines **102***a*, **102***b* electrically coupled to a common DQ line **112** and their DQS data strobe signal lines **104***a*, **104***b* electrically coupled to a common DQS line **114**. The common DQ line **112** and the common DQS line **114** are electrically coupled to the memory controller **20** of the computer system. Thus, the computer system is exposed to the loads of both memory devices **30***a*, **30***b* concurrently.

In certain embodiments, the circuit **40** selectively isolates the loads of at least some of the memory devices **30** from the computer system. The circuit **40** of certain embodiments is configured to present a significantly reduced load to the computer system. In certain embodiments in which the memory devices **30** are arranged in a plurality of ranks, the circuit **40** selectively isolates the loads of some (e.g., one or more) of the ranks of the memory module **10** from the computer system. In certain other embodiments, the circuit **40** selectively isolates the loads of all of the ranks of the memory module **10** from the computer system. For example, when a memory module **10** is not being accessed by the computer system, the capacitive load on the memory controller **20** of the computer system by the memory module **10** can be substantially reduced to the capacitive load of the circuit **40** of the memory module **10**.

As schematically illustrated by FIGS. **3**A and **3**B, an example memory module **10** compatible with certain embodiments described herein comprises a circuit **40** which selectively isolates one or both of the DQ data signal lines **102***a*, **102***b* of the two memory devices **30***a*, **30***b* from the common DQ data signal line **112** coupled to the computer system. Thus, the circuit **40** selectively allows a DQ data signal to be transmitted from the memory controller **20** of the computer system to one or both of the DQ data signal lines **102***a*, **102***b*. In addition, the circuit **40** selectively allows one of a first DQ data signal from the DQ data signal line **102***a* of the first memory device **30***a* or a second DQ data signal from the DQ data signal line **102***b* of the second memory device **30***b* to be transmitted to the memory controller **20** via the common DQ data signal line **112** (see. e.g., triangles on the DQ and DQS lines of FIGS. **3**A and **3**B which point towards the memory controller). While various figures of the present application denote read operations by use of DQ and DQS lines which have triangles pointing towards the memory controller, certain embodiments described herein are also compatible with write operations (e.g., as would be denoted by triangles on the DQ or DQS lines pointing away from the memory controller).

For example, in certain embodiments, the circuit **40** comprises a pair of switches **120***a*, **120***b* on the DQ data signal lines **102***a*, **102***b* as schematically illustrated by FIG. **3**A. Each switch **120***a*, **120***b* is selectively actuated to selectively electrically couple the DQ data signal line **102***a* to the common DQ signal line **112**, the DQ data signal line **102***b* to the common DQ signal line **112**, or both DQ data signal lines **102***a*, **102***b* to the common DQ signal line **112**. In certain other embodiments, the circuit **40** comprises a switch **120** electrically coupled to both of the DQ data signal lines **102***a*, **102***b*, as schematically illustrated by FIG. **3**B. The switch **120** is selectively actuated to selectively electrically couple the DQ data signal line **102***a* to the common DQ signal line **112**, the DQ data signal line **102***b* to the common DQ signal line **112**, or both DQ signal lines **102***a*, **102***b* to the common DQ signal line **112**. Circuits **40** having other configurations of switches are also compatible with embodiments described herein. While each of the memory devices **30***a*, **30***b* has a plurality of DQ data signal lines and a plurality of DQS data strobe signal lines, FIGS. **3**A and **3**B only illustrate a single DQ data signal line and a single DQS data strobe signal line for each memory device **30***a*, **30***b* for simplicity. The configurations schematically illustrated by FIGS. **3**A and **3**B can be applied to all of the DQ data signal lines and DQS data strobe signal lines of the memory module **10**.

In certain embodiments, the circuit **40** selectively isolates the loads of ranks of memory devices **30** from the computer system. As schematically illustrated in FIGS. **4**A and **4**B, example memory modules **10** compatible with certain embodiments described herein comprise a first number of memory devices **30** arranged in a first number of ranks **32**. The memory modules **10** of FIGS. **4**A and **4**B comprises two ranks **32***a*, **32***b*, with each rank **32***a*, **32***b* having a corresponding set of DQ data signal lines and a corresponding set of DQS data strobe lines. Other numbers of ranks (e.g., four ranks) of memory devices **30** of the memory module **10** are also compatible with certain embodiments described herein. For simplicity, FIGS. **4**A and **4**B illustrate only a single DQ data signal line and a single DQS data strobe signal line from each rank **32**.

The circuit **40** of FIG. **4**A selectively isolates one or more of the DQ data signal lines **102***a*, **102***b* of the two ranks **32***a*, **32***b* from the computer system. Thus, the circuit **40** selectively allows a DQ data signal to be transmitted from the memory controller **20** of the computer system to the memory devices **30** of one or both of the ranks **32***a*, **32***b* via the DQ

data signal lines **102***a*, **102***b*. In addition, the circuit **40** selectively allows one of a first DQ data signal from the DQ data signal line **102***a* of the first rank **32***a* and a second DQ data signal from the DQ data signal line **102***b* of the second rank **32***b* to be transmitted to the memory controller **20** via the common DQ data signal line **112**. For example, in certain embodiments, the circuit **40** comprises a pair of switches **120***a*, **120***b* on the DQ data signal lines **102***a*, **102***b* as schematically illustrated by FIG. **4**A. Each switch **120***a*, **120***b* is selectively actuated to selectively electrically couple the DQ data signal line **102***a* to the common DQ data signal line **112**, the DQ data signal line **102***b* to the common DQ data signal line **112**, or both DQ data signal lines **102***a*, **102***b* to the common DQ data signal line **112**. In certain other embodiments, the circuit **40** comprises a switch **120** electrically coupled to both of the DQ data signal lines **102***a*, **102***b*, as schematically illustrated by FIG. **4**B. The switch **120** is selectively actuated to selectively electrically couple the DQ data signal line **102***a* to the common DQ data signal line **112**, the DQ data signal line **102***b* to the common DQ data signal line **112**, or both DQ data signal lines **102***a*, **102***b* to the common DQ data signal line **112**. Circuits **40** having other configurations of switches are also compatible with embodiments described herein.

In the example embodiments schematically illustrated by FIGS. **3**A, **3**B, **4**A, and **4**B, the circuit **40** comprises a logic element which is integral with and comprises the switches **120** which are coupled to the DQ data signal lines and the DQS data strobe signal lines. In certain such embodiments, each switch **120** comprises a data path multiplexer/demultiplexer. In certain other embodiments, the circuit **40** comprises a logic element **122** which is a separate component operatively coupled to the switches **120**, as schematically illustrated by FIGS. **5**A-**5**D. The one or more switches **120** are operatively coupled to the logic element **122** to receive control signals from the logic element **122** and to selectively electrically couple one or more data signal lines to a common data signal line. Example switches compatible with embodiments described herein include, but are not limited to field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Tex. Example logic elements **122** compatible with certain embodiments described herein include, but are not limited to, programmable-logic devices (PLD), application-specific integrated circuits (ASIC), field-programmable gate arrays (FPGA), custom-designed semiconductor devices, and complex programmable-logic devices (CPLD). Example logic elements **122** are available from Lattice Semiconductor Corporation of Hillsboro, Oreg., Altera Corporation of San Jose, Calif., and Xilinx Incorporated of San Jose, Calif.

In certain embodiments, the load isolation provided by the circuit **40** advantageously allows the memory module **10** to present a reduced load (e.g., electrical load, such as capacitive load, inductive load, or impedance load) to the computer system by selectively switching between the two ranks of memory devices **30** to which it is coupled. This feature is used in certain embodiments in which the load of the memory module **10** may otherwise limit the number of ranks or the number of memory devices per memory module. In certain embodiments, the memory module **10** operates as having a data path rank buffer which advantageously isolates the ranks of memory devices **30** of the memory module **10** from one another, from the ranks on other memory modules, and from the computer system. This data path rank buffer of certain embodiments advantageously provides DQ-DQS paths for each rank or sets of ranks of memory devices which are separate from one another, or which are separate from the memory controller of the computer system. In certain embodiments, the load isolation advantageously diminishes the effects of capacitive loading, jitter and other sources of noise. In certain embodiments, the load isolation advantageously simplifies various other aspects of operation of the memory module **10**, including but not limited to, setup-and-hold time, clock skew, package skew, and process, temperature, voltage, and transmission line variations.

For certain memory module applications that utilize multiple ranks of memory, increased load on the memory bus can degrade speed performance. In certain embodiments described herein, selectively isolating the loads of the ranks of memory devices **30** advantageously decreases the load on the computer system, thereby allowing the computer system (e.g., server) to run faster with improved signal integrity. In certain embodiments, load isolation advantageously provides system memory with reduced electrical loading, thereby improving the electrical topology to the memory controller **20**. In certain such embodiments, the speed and the memory density of the computer system are advantageously increased without sacrificing one for the other.

In certain embodiments, load isolation advantageously increases the size of the memory array supported by the memory controller **20** of the computer system. The larger memory array has an increased number of memory devices **30** and ranks of memory devices **30** of the memory module **10**, with a corresponding increased number of chip selects. Certain embodiments described herein advantageously provide more system memory using fewer chip selects, thereby avoiding the chip select limitation of the memory controller.

An exemplary section of Verilog code corresponding to logic compatible with a circuit **40** which provides load isolation is listed below in Example 1. The exemplary code of Example 1 corresponds to a circuit **40** comprising six FET switches for providing load isolation to DQ and DQS lines.

Example 1

```
//========================== declarations
  reg          rasN_R, casN_R, weN_R;
  wire         actv_cmd_R, pch_cmd_R, pch_all_cmd_R, ap_xfr_cmd_R_R;
  wire         xfr_cmd_R,mrs_cmd,rd_cmd_R;
  //- - - - - - - - - - - - - - - - - - - - - - - - DDR 2 FET
  reg          brs0N_R;                  // registered chip sel
  reg          brs1N_R;                  // registered chip sel
  reg          brs2N_R;                  // registered chip sel
  reg          brs3N_R;                  // registered chip sel
  wire         sel;
  wire         sel_01;
  wire         sel_23;
  wire         rd_R1;
```

-continued

```
  wire                  wr_cmd_R,wr_R1;
  reg                   rd_R2,rd_R3,rd_R4,rd_R5;
  reg                   wr_R2,wr_R3,wr_R4,wr_R5;
  reg                   enfet1,enfet2,enfet3,enfet4,enfet5,enfet6;
  wire                  wr_01_R1,wr_23_R1;
  reg                   wr_01_R2,wr_01_R3,wr_01_R4;
  reg                   wr_23_R2,wr_23_R3,wr_23_R4;
  wire                  rodt0_a,rodt0_b;
//========================== logic
  always @(posedge clk_in)
          begin
                  brs0N_R <= brs0_in_N;     // cs0
                  brs1N_R <= brs1_in_N;     // cs1
                  brs2N_R <= brs2_in_N;     // cs2
                  brs3N_R <= brs3_in_N;     // cs3
                  rasN_R <= brras_in_N ;
                  casN_R <= brcas_in_N ;
                  weN_R <= bwe_in_N ;
          end
assign sel = ~brs0N_R | ~brs1N_R | ~brs2N_R | ~brs3N_R ;
assign sel_01 = ~brs0N_R | ~brs1N_R ;
assign sel_23 = ~brs2N_R | ~brs3N_R ;
assign actv_cmd_R = !rasN_R & casN_R & weN_R; // activate cmd
assign pch_cmd_R = !rasN_R & casN_R & !weN_R ;// pchg cmd
assign xfr_cmd_R = rasN_R & !casN_R;                // xfr cmd
assign mrs_cmd = !rasN_R & !casN_R & !weN_R ;   // md reg set cmd
assign rd_cmd_R = rasN_R & !casN_R & weN_R ;   // read cmd
assign wr_cmd_R = rasN_R & !casN_R & !weN_R ;  // write cmd
//---------------------------------------
assign    rd_R1 = sel & rd_cmd_R;  // rd cmd cyc 1
assign    wr_R1 = sel & wr_cmd_R; // wr cmd cyc 1
//---------------------------------------
  always @(posedge clk_in)
          begin
                  rd_R2 <= rd_R1 ;
                  rd_R3 <= rd_R2;
                  rd_R4 <= rd_R3;
                  rd_R5 <= rd_R4;
//                rd0_o_R6 <= rd0_o_R5;
                  wr_R2 <= wr_R1 ;
                  wr_R3 <= wr_R2;
                  wr_R4 <= wr_R3;
                  wr_R5 <= wr_R4;
          end
//---------------------------------------
assign    wr_01_R1 = sel_01 & wr_cmd_R; // wr cmd cyc 1 for cs 2 & cs3
assign    wr_23_R1 = sel_23 & wr_cmd_R; // wr cmd cyc 1 for cs 2 & cs3
  always @(posedge clk_in)
          begin
                  wr_01_R2 <= wr_01_R1 ;
                  wr_01_R3 <= wr_01_R2;
                  wr_01_R4 <= wr_01_R3;
                  wr_23_R2 <= wr_23_R1 ;
                  wr_23_R3 <= wr_23_R2;
                  wr_23_R4 <= wr_23_R3;
          end
assign    rodt0_ab = (rodt0)          // odt cmd from sys
                  | (wr_23_R1)  // wr 1st cyc to other rnks (assume single dimm per channel)
                  | (wr_23_R2)  // wr 2nd cyc to other rnks (assume single dimm per channel)
                  | (wr_23_R3)  // wr 3rd cyc to other rnks (assume single dimm per channel)
                  ;
assign    rodt1_ab = (rodt1)          // odt cmd from sys
                  | (wr_01_R1)  // wr 1st cyc to other rnks (assume single dimm per channel)
                  | (wr_01_R2)  // wr 2nd cyc to other rnks (assume single dimm per channel)
                  | (wr_01_R3)  // wr 3rd cyc to other rnks (assume single dimm per channel)
                  ;
//---------------------------------------
  always @(posedge clk_in)
          begin
   if (
     | (rd_R2)                          // pre-am rd
     | (rd_R3)                          // 1st cyc of rd brst (cl3)
     | (rd_R4)                          // 2nd cyc of rd brst (cl3)
     | (wr_R1)                          // pre-am wr
     | (wr_R2)                          // wr brst 1st cyc
     | (wr_R3)                          // wr brst 2nd cyc
     ) begin
                  enfet1 <= 1'b1;       // enable fet
                  enfet2 <= 1'b1;       // enable fet
```

-continued

```
                enfet3 <= 1'b1;        // enable fet
                enfet4 <= 1'b1;        // enable fet
                enfet5 <= 1'b1;        // enable fet
                enfet6 <= 1'b1;        // enable fet
        end
    else
        begin
                enfet1 <= 1'b0;        // disable fet
                enfet2 <= 1'b0;        // disable fet
                enfet3 <= 1'b0;        // disable fet
                enfet4 <= 1'b0;        // disable fet
                enfet5 <= 1'b0;        // disable fet
                enfet6 <= 1'b0;        // disable fet
        end
end
```

Back-to-Back Adjacent Read Commands

Due to their source synchronous nature, DDR SDRAM (e.g., DDR1, DDR2, DDR3) memory devices operate with a data transfer protocol which surrounds each burst of data strobes with a pre-amble time interval and a post-amble time interval. The pre-amble time interval provides a timing window for the receiving memory device to enable its data capture circuitry when a known valid level is present on the strobe signal to avoid false triggers of the memory device's capture circuit. The post-amble time interval provides extra time after the last strobe for this data capture to facilitate good signal integrity. In certain embodiments, when the computer system accesses two consecutive bursts of data from the same memory device, termed herein as a "back-to-back adjacent read," the post-amble time interval of the first read command and the pre-amble time interval of the second read command are skipped by design protocol to increase read efficiency. FIG. **6A** shows an exemplary timing diagram of this "gapless" read burst for a back-to-back adjacent read condition from one memory device.

In certain embodiments, when the second read command accesses data from a different memory device than does the first read command, there is at least one time interval (e.g., clock cycle) inserted between the data strobes of the two memory devices. This inserted time interval allows both read data bursts to occur without the post-amble time interval of the first read data burst colliding or otherwise interfering with the pre-amble time interval of the second read data burst. In certain embodiments, the memory controller of the computer system inserts an extra clock cycle between successive read commands issued to different memory devices, as shown in the exemplary timing diagram of FIG. **6B** for successive read accesses from different memory devices.

In typical computer systems, the memory controller is informed of the memory boundaries between the ranks of memory of the memory module prior to issuing read commands to the memory module. Such memory controllers can insert wait time intervals or clock cycles to avoid collisions or interference between back-to-back adjacent read commands which cross memory device boundaries, which are referred to herein as "BBARX."

In certain embodiments described herein in which the number of ranks **32** of the memory module **10** is doubled or quadrupled, the circuit **40** generates a set of output address and command signals so that the selection decoding is transparent to the computer system. However, in certain such embodiments, there are memory device boundaries of which the computer system is unaware, so there are occasions in which BBARX occurs without the cognizance of the memory controller **20** of the computer system. As shown in FIG. **7**, the last data strobe of memory device "a" collides with the pre-amble time interval of the data strobe of memory device "b," resulting in a "collision window."

FIGS. **8A-8**D schematically illustrate circuit diagrams of example memory modules **10** comprising a circuit **40** which multiplexes the DQS data strobe signal lines **104***a*, **104***b* of two ranks **32***a*, **32***b* from one another in accordance with certain embodiments described herein. While the DQS data strobe signal lines **104***a*, **104***b* of FIGS. **8A-8**D correspond to two ranks **32***a*, **32***b* of memory devices **30**, in certain other embodiments, the circuit **40** multiplexes the DQS data strobe signal lines **104***a*, **104***b* corresponding to two individual memory devices **30***a*, **30***b*.

FIG. **8A** schematically illustrates a circuit diagram of an exemplary memory module **10** comprising a circuit **40** in accordance with certain embodiments described herein. In certain embodiments, BBARX collisions are avoided by a mechanism which electrically isolates the DQS data strobe signal lines **104***a*, **104***b* from one another during the transition from the first read data burst of one rank **32***a* of memory devices **30** to the second read data burst of another rank **32***b* of memory devices **30**.

In certain embodiments, as schematically illustrated by FIG. **8A**, the circuit **40** comprises a first switch **130***a* electrically coupled to a first DQS data strobe signal line **104***a* of a first rank **32***a* of memory devices **30** and a second switch **130***b* electrically coupled to a second DQS data strobe signal line **104***b* of a second rank **32***b* of memory devices **30**. In certain embodiments, the time for switching the first switch **130***a* and the second switch **130***b* is between the two read data bursts (e.g., after the last DQS data strobe of the read data burst of the first rank **32***a* and before the first DQS data strobe of the read data burst of the second rank **32***b*). During the read data burst for the first rank **32***a*, the first switch **130***a* is enabled. After the last DQS data strobe of the first rank **32***a* and before the first DQS data strobe of the second rank **32***b*, the first switch **130***a* is disabled and the second switch **130***b* is enabled.

As shown in FIG. **8A**, each of the ranks **32***a*, **32***b* otherwise involved in a BBARX collision have their DQS data strobe signal lines **104***a*, **104***b* selectively electrically coupled to the common DQS line **114** through the circuit **40**. The circuit **40** of certain embodiments multiplexes the DQS data strobe signal lines **104***a*, **104***b* of the two ranks **32***a*, **32***b* of memory devices **30** from one another to avoid a BBARX collision.

In certain embodiments, as schematically illustrated by FIG. **8B**, the circuit **40** comprises a switch **130** which multiplexes the DQS data strobe signal lines **104***a*, **104***b*

from one another. For example, the circuit **40** receives a DQS data strobe signal from the common DQS data strobe signal line **114** and selectively transmits the DQS data strobe signal to the first DQS data strobe signal line **104***a*, to the second DQS data strobe signal line **104***b*, or to both DQS data strobe signal lines **104***a*, **104***b*. As another example, the circuit **40** receives a first DQS data strobe signal from the first rank **32***a* of memory devices **30** and a second DQS data strobe signal from a second rank **32***b* of memory devices **30** and selectively switches one of the first and second DQS data strobe signals to the common DQS data strobe signal line **114**.

In certain embodiments, the circuit **40** also provides the load isolation described above in reference to FIGS. **1-5**. For example, as schematically illustrated by FIG. **8**C, the circuit **40** comprises both the switch **120** for the DQ data signal lines **102***a*, **102***b* and the switch **130** for the DQS data strobe signal lines **104***a*, **104***b*. While in certain embodiments, the switches **130** are integral with a logic element of the circuit **40**, in certain other embodiments, the switches **130** are separate components which are operatively coupled to a logic element **122** of the circuit **40**, as schematically illustrated by FIG. **8**D. In certain such embodiments, the control and timing of the switch **130** is performed by the circuit **40** which is resident on the memory module **10**. Example switches **130** compatible with embodiments described herein include, but are not limited to field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Tex., and multiplexers, such as the SN74AUC2G53 2:1 analog multiplexer/demultiplexer available from Texas Instruments. Inc. of Dallas, Tex.

The circuit **40** of certain embodiments controls the isolation of the DQS data strobe signal lines **104***a*, **104***b* by monitoring commands received by the memory module **10** from the computer system and producing "windows" of operation whereby the appropriate switches **130** are activated or deactivated to enable and disable the DQS data strobe signal lines **104***a*, **104***b* to mitigate BBARX collisions. In certain other embodiments, the circuit **40** monitors the commands received by the memory module **10** from the computer system and selectively activates or deactivates the switches **120** to enable and disable the DQ data signal lines **102***a*, **102***b* to reduce the load of the memory module **10** on the computer system. In still other embodiments, the circuit **40** performs both of these functions together.

Command Signal Translation

Most high-density memory modules are currently built with 512-Megabit ("512-Mb") memory devices wherein each memory device has a 64 M×8-bit configuration. For example, a 1-Gigabyte ("1-GB") memory module with error checking capabilities can be fabricated using eighteen such 512-Mb memory devices. Alternatively, it can be economically advantageous to fabricate a 1-GB memory module using lower-density memory devices and doubling the number of memory devices used to produce the desired word width. For example, by fabricating a 1-GB memory module using thirty-six 256-Mb memory devices with 64 M×4-bit configuration, the cost of the resulting 1-GB memory module can be reduced since the unit cost of each 256-Mb memory device is typically lower than one-half the unit cost of each 512-Mb memory device. The cost savings can be significant, even though twice as many 256-Mb memory devices are used in place of the 512-Mb memory devices. For example, by using pairs of 512-Mb memory devices rather than single 1-Gb memory devices, certain embodiments described herein reduce the cost of the memory module by a factor of up to approximately five.

Market pricing factors for DRAM devices are such that higher-density DRAM devices (e.g., 1-Gb DRAM devices) are much more than twice the price of lower-density DRAM devices (e.g., 512-Mb DRAM devices). In other words, the price per bit ratio of the higher-density DRAM devices is greater than that of the lower-density DRAM devices. This pricing difference often lasts for months or even years after the introduction of the higher-density DRAM devices, until volume production factors reduce the costs of the newer higher-density DRAM devices. Thus, when the cost of a higher-density DRAM device is more than the cost of two lower-density DRAM devices, there is an economic incentive for utilizing pairs of the lower-density DRAM devices to replace individual higher-density DRAM devices.

FIG. **9**A schematically illustrates an exemplary memory module **10** compatible with certain embodiments described herein. The memory module **10** is connectable to a memory controller **20** of a computer system (not shown). The memory module **10** comprises a printed circuit board **210** and a plurality of memory devices **30** coupled to the printed circuit board **210**. The plurality of memory devices **30** has a first number of memory devices **30**. The memory module **10** further comprises a circuit **40** coupled to the printed circuit board **210**. The circuit **40** receives a set of input address and command signals from the computer system. The set of input address and command signals correspond to a second number of memory devices **30** smaller than the first number of memory devices **30**. The circuit **40** generates a set of output address and command signals in response to the set of input address and command signals. The set of output address and command signals corresponds to the first number of memory devices **30**.

In certain embodiments, as schematically illustrated in FIG. **9**A, the memory module **10** further comprises a phase-lock loop device **220** coupled to the printed circuit board **210** and a register **230** coupled to the printed circuit board **210**. In certain embodiments, the phase-lock loop device **220** and the register **230** are each mounted on the printed circuit board **210**. In response to signals received from the computer system, the phase-lock loop device **220** transmits clock signals to the plurality of memory devices **30**, the circuit **40**, and the register **230**. The register **230** receives and buffers a plurality of command signals and address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals), and transmits corresponding signals to the appropriate memory devices **30**. In certain embodiments, the register **230** comprises a plurality of register devices. While the phase-lock loop device **220**, the register **230**, and the circuit **40** are described herein in certain embodiments as being separate components, in certain other embodiments, two or more of the phase-lock loop device **220**, the register **230**, and the circuit **40** are portions of a single component. Persons skilled in the art are able to select a phase-lock loop device **220** and a register **230** compatible with embodiments described herein.

In certain embodiments, the memory module **10** further comprises electrical components which are electrically coupled to one another and are surface-mounted or embedded on the printed circuit board **210**. These electrical components can include, but are not limited to, electrical conduits, resistors, capacitors, inductors, and transistors. In certain embodiments, at least some of these electrical components are discrete, while in other certain embodiments, at

least some of these electrical components are constituents of one or more integrated circuits.

In certain embodiments, the printed circuit board **210** is mountable in a module slot of the computer system. The printed circuit board **210** of certain such embodiments has a plurality of edge connections electrically coupled to corresponding contacts of the module slot and to the various components of the memory module **10**, thereby providing electrical connections between the computer system and the components of the memory module **10**.

In certain embodiments, the plurality of memory devices **30** are arranged in a first number of ranks **32**. For example, in certain embodiments, the memory devices **30** are arranged in four ranks **32***a*, **32***b*, **32***c*, **32***d*, as schematically illustrated by FIG. **9**A. In certain other embodiments, the memory devices **30** are arranged in two ranks **32***a*, **32***b*, as schematically illustrated by FIG. **9**B. Other numbers of ranks **32** of the memory devices **30** are also compatible with embodiments described herein.

As schematically illustrated by FIGS. **9**A and **9**B, in certain embodiments, the circuit **40** receives a set of input command signals (e.g., refresh, precharge) and address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals) from the memory controller **20** of the computer system. In response to the set of input address and command signals, the circuit **40** generates a set of output address and command signals.

In certain embodiments, the set of output address and command signals corresponds to a first number of ranks in which the plurality of memory devices **30** of the memory module **10** are arranged, and the set of input address and command signals corresponds to a second number of ranks per memory module for which the computer system is configured. The second number of ranks in certain embodiments is smaller than the first number of ranks. For example, in the exemplary embodiment as schematically illustrated by FIG. **9**A, the first number of ranks is four while the second number of ranks is two. In the exemplary embodiment of FIG. **9**B, the first number of ranks is two while the second number of ranks is one. Thus, in certain embodiments, even though the memory module **10** actually has the first number of ranks of memory devices **30**, the memory module **10** simulates a virtual memory module by operating as having the second number of ranks of memory devices **30**. In certain embodiments, the memory module **10** simulates a virtual memory module when the number of memory devices **30** of the memory module **10** is larger than the number of memory devices **30** per memory module for which the computer system is configured to utilize. In certain embodiments, the circuit **40** comprises logic (e.g., address decoding logic, command decoding logic) which translates between a system memory domain of the computer system and a physical memory domain of the memory module **10**.

In certain embodiments, the computer system is configured for a number of ranks per memory module which is smaller than the number of ranks in which the memory devices **30** of the memory module **10** are arranged. In certain such embodiments, the computer system is configured for two ranks of memory per memory module (providing two chip-select signals CS_0, CS_1) and the plurality of memory modules **30** of the memory module **10** are arranged in four ranks, as schematically illustrated by FIG. **9**A. In certain other such embodiments, the computer system is configured for one rank of memory per memory module (providing one chip-select signal CS_0) and the plurality of memory modules **30** of the memory module **10** are arranged in two ranks, as schematically illustrated by FIG. **9**B.

In the exemplary embodiment schematically illustrated by FIG. **9**A, the memory module **10** has four ranks of memory devices **30** and the computer system is configured for two ranks of memory devices per memory module. The memory module **10** receives row/column address signals or signal bits (A_0-A_{n+1}), bank address signals (BA_0-BA_m), chip-select signals (CS_0 and CS_1), and command signals (e.g., refresh, precharge, etc.) from the computer system. The A_0-A_n row/column address signals are received by the register **230**, which buffers these address signals and sends these address signals to the appropriate ranks of memory devices **30**. The circuit **40** receives the two chip-select signals (CS_0, CS_1) and one row/column address signal (A_{n+1}) from the computer system. Both the circuit **40** and the register **230** receive the bank address signals (BA_0-BA_m) and at least one command signal (e.g., refresh, precharge, etc.) from the computer system.

Logic Tables

Table 1 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices **30** using chip-select signals.

TABLE 1

State	CS_0	CS_1	A_{n+1}	Command	CS_{0A}	CS_{0B}	CS_{1A}	CS_{1B}
1	0	1	0	Active	0	1	1	1
2	0	1	1	Active	1	0	1	1
3	0	1	x	Active	0	0	1	1
4	1	0	0	Active	1	1	0	1
5	1	0	1	Active	1	1	1	0
6	1	0	x	Active	1	1	0	0
7	1	1	x	x	1	1	1	1

Note:
1. CS_0, CS_1, CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are active low signals.
2. A_{n+1} is an active high signal.
3. 'x' is a Don't Care condition.
4. Command involves a number of command signals that define operations such as refresh, precharge, and other operations.

In Logic State 1: CS_0 is active low, A_{n+1} is non-active, and Command is active. CS_{0A} is pulled low, thereby selecting Rank 0.

In Logic State 2: CS_0 is active low, A_{n+1} is active, and Command is active. CS_{0B} is pulled low, thereby selecting Rank 1.

In Logic State 3: CS_0 is active low. A_{n+1} is Don't Care, and Command is active high. CS_{0A} and CS_{0B} are pulled low, thereby selecting Ranks 0 and 1.

In Logic State 4: CS_1 is active low, A_{n+1} is non-active, and Command is active. CS_{1A} is pulled low, thereby selecting Rank 2.

In Logic State 5: CS_1 is active low, A_{n+1} is active, and Command is active. CS_{1B} is pulled low, thereby selecting Rank 3.

In Logic State 6: CS_1 is active low, A_{n+1} is Don't Care, and Command is active. CS_{1A} and CS_1B are pulled low, thereby selecting Ranks 2 and 3.

In Logic State 7: CS_0 and CS_1 are pulled non-active high, which deselects all ranks, i.e., CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are pulled high.

The "Command" column of Table 1 represents the various commands that a memory device (e.g., a DRAM device) can execute, examples of which include, but are not limited to, activation, read, write, precharge, and refresh. In certain embodiments, the command signal is passed through to the selected rank only (e.g., state 4 of Table 1). In such embodiments, the command signal (e.g., read) is sent to only one

memory device or the other memory device so that data is supplied from one memory device at a time. In other embodiments, the command signal is passed through to both associated ranks (e.g., state 6 of Table 1). In such embodiments, the command signal (e.g., refresh) is sent to both memory devices to ensure that the memory content of the memory devices remains valid over time. Certain embodiments utilize a logic table such as that of Table 1 to simulate a single memory device from two memory devices by selecting two ranks concurrently.

Table 2 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices **30** using gated CAS signals.

TABLE 2

CS*	RAS*	CAS*	WE*	Density Bit	A_{10}	Command	CAS0*	CAS1*
1	x	x	x	x	x	NOP	x	x
0	1	1	1	x	x	NOP	1	1
0	0	1	1	0	x	ACTIVATE	1	1
0	0	1	1	1	x	ACTIVATE	1	1
0	1	0	1	0	x	READ	0	1
0	1	0	1	1	x	READ	1	0
0	1	0	0	0	x	WRITE	0	1
0	1	0	0	1	x	WRITE	1	0
0	0	1	0	0	0	PRECHARGE	1	1
0	0	1	0	1	0	PRECHARGE	1	1
0	0	1	0	x	1	PRECHARGE	1	1
0	0	0	0	x	x	MODE REG SET	0	0
0	0	0	1	x	x	REFRESH	0	0

In certain embodiments in which the density bit is a row address bit, for read/write commands, the density bit is the value latched during the activate command for the selected bank.

Serial-Presence-Detect Device

Memory modules typically include a serial-presence detect (SPD) device **240** (e.g., an electrically-erasable-programmable read-only memory or EEPROM device) comprising data which characterize various attributes of the memory module, including but not limited to, the number of row addresses the number of column addresses, the data width of the memory devices, the number of ranks, the memory density per rank, the number of memory devices, and the memory density per memory device. The SPD device **240** communicates this data to the basic input/output system (BIOS) of the computer system so that the computer system is informed of the memory capacity and the memory configuration available for use and can configure the memory controller properly for maximum reliability and performance.

For example, for a commercially-available 512-MB (64 M×8-byte) memory module utilizing eight 512-Mb memory devices each with a 64 M×8-bit configuration, the SPD device contains the following SPD data (in appropriate bit fields of these bytes):

Byte 3: Defines the number of row address bits in the DRAM device in the memory module [13 for the 512-Mb memory device].

Byte 4: Defines the number of column address bits in the DRAM device in the memory module [11 for the 512-Mb memory device].

Byte 13: Defines the bit width of the primary DRAM device used in the memory module [8 bits for the 512-Mb (64 M×8-bit) memory device].

Byte 14: Defines the bit width of the error checking DRAM device used in the memory module [8 bits for the 512-Mb (64 M×8-bit) memory device].

Byte 17: Defines the number of banks internal to the DRAM device used in the memory module [4 for the 512-Mb memory device].

In a further example, for a commercially-available 1-GB (128 M×8-byte) memory module utilizing eight 1-Gb memory devices each with a 128 M×8-bit configuration, as described above, the SPD device contains the following SPD data (in appropriate bit fields of these bytes):

Byte 3: Defines the number of row address bits in the DRAM device in the memory module [14 for the 1-Gb memory device].

Byte 4: Defines the number of column address bits in the DRAM device in the memory module [11 for the 1-Gb memory device].

Byte 13: Defines the bit width of the primary DRAM device used in the memory module [8 bits for the 1-Gb (128 M×8-bit) memory device].

Byte 14: Defines the bit width of the error checking DRAM device used in the memory module [8 bits for the 1-Gb (128 M×8-bit) memory device].

Byte 17: Defines the number of banks internal to the DRAM device used in the memory module [4 for the 1-Gb memory device].

In certain embodiments, the SPD device **240** comprises data which characterize the memory module **10** as having fewer ranks of memory devices than the memory module **10** actually has, with each of these ranks having more memory density. For example, for a memory module **10** compatible with certain embodiments described herein having two ranks of memory devices **30**, the SPD device **240** comprises data which characterizes the memory module **10** as having one rank of memory devices with twice the memory density per rank. Similarly, for a memory module **10** compatible with certain embodiments described herein having four ranks of memory devices **30**, the SPD device **240** comprises data which characterizes the memory module **10** as having two ranks of memory devices with twice the memory density per rank. In addition, in certain embodiments, the SPD device **240** comprises data which characterize the memory module **10** as having fewer memory devices than the memory module **10** actually has, with each of these memory devices having more memory density per memory device. For example, for a memory module **10** compatible with certain embodiments described herein, the SPD device **240** comprises data which characterizes the memory module **10** as having one-half the number of memory devices that the

memory module **10** actually has, with each of these memory devices having twice the memory density per memory device. Thus, in certain embodiments, the SPD device **240** informs the computer system of the larger memory array by reporting a memory device density that is a multiple of the memory devices **30** resident on the memory module **10**. Certain embodiments described herein advantageously do not require system level changes to hardware (e.g., the motherboard of the computer system) or to software (e.g., the BIOS of the computer system).

FIG. **9**C schematically illustrates an exemplary memory module **10** in accordance with certain embodiments described herein. The memory module **10** comprises a pair of substantially identical memory devices **31**, **33**. Each memory device **31**, **33** has a first bit width, a first number of banks of memory locations, a first number of rows of memory locations, and a first number of columns of memory locations. The memory module **10** further comprises an SPD device **240** comprising data that characterizes the pair of memory devices **31**, **33**. The data characterize the pair of memory devices **31**, **33** as a virtual memory device having a second bit width equal to twice the first bit width, a second number of banks of memory locations equal to the first number of banks, a second number of rows of memory locations equal to the first number of rows, and a second number of columns of memory locations equal to the first number of columns.

In certain such embodiments, the SPD device **240** of the memory module **10** is programmed to describe the combined pair of lower-density memory devices **31**, **33** as one virtual or pseudo-higher-density memory device. In an exemplary embodiment, two 512-Mb memory devices, each with a 128 M×**4**-bit configuration, are used to simulate one 1-Gb memory device having a 128 M×8-bit configuration. The SPD device **240** of the memory module **10** is programmed to describe the pair of 512-Mb memory devices as one virtual or pseudo-1-Gb memory device.

For example, to fabricate a 1-GB (128 M×8-byte) memory module, sixteen 512-Mb (128 M×**4**-bit) memory devices can be used. The sixteen 512-Mb (128 M×**4**-bit) memory devices are combined in eight pairs, with each pair serving as a virtual or pseudo-1-Gb (128 M×8-bit) memory device. In certain such embodiments, the SPD device **240** contains the following SPD data (in appropriate bit fields of these bytes):

Byte 3: 13 row address bits.

Byte **4**: 12 column address bits.

Byte 13: 8 bits wide for the primary virtual 1-Gb (128 M×8-bit) memory device.

Byte **14**: 8 bits wide for the error checking virtual 1-Gb (128 M×8-bit) memory device.

Byte 17: 4 banks.

In this exemplary embodiment, bytes 3, 4, and 17 are programmed to have the same values as they would have for a 512-MB (128 M×4-byte) memory module utilizing 512-Mb (128 M×**4**-bit) memory devices. However, bytes 13 and 14 of the SPD data are programmed to be equal to 8, corresponding to the bit width of the virtual or pseudo-higher-density 1-Gb (128 M×8-bit) memory device, for a total capacity of 1-GB. Thus, the SPD data does not describe the actual-lower-density memory devices, but instead describes the virtual or pseudo-higher-density memory devices. The BIOS accesses the SPD data and recognizes the memory module as having 4 banks of memory locations arranged in 2^{13} rows and 2^{12} columns, with each memory location having a width of 8 bits rather than **4** bits.

In certain embodiments, when such a memory module **10** is inserted in a computer system, the computer system's memory controller then provides to the memory module **10** a set of input address and command signals which correspond to the number of ranks or the number of memory devices reported by the SPD device **240**. For example, placing a two-rank memory module **10** compatible with certain embodiments described herein in a computer system compatible with one-rank memory modules, the SPD device **240** reports to the computer system that the memory module **10** only has one rank. The circuit **40** then receives a set of input address and command signals corresponding to a single rank from the computer system's memory controller, and generates and transmits a set of output address and command signals corresponding to two ranks to the appropriate memory devices **30** of the memory module **10**.

Similarly, when a two-rank memory module **10** compatible with certain embodiments described herein is placed in a computer system compatible with either one- or two-rank memory modules, the SPD device **240** reports to the computer system that the memory module **10** only has one rank. The circuit **40** then receives a set of input address and command signals corresponding to a single rank from the computer system's memory controller, and generates and transmits a set of output address and command signals corresponding to two ranks to the appropriate memory devices **30** of the memory module **10**.

Furthermore, a four-rank memory module **10** compatible with certain embodiments described herein simulates a two-rank memory module whether the memory module **10** is inserted in a computer system compatible with two-rank memory modules or with two- or four-rank memory modules. Thus, by placing a four-rank memory module **10** compatible with certain embodiments described herein in a module slot that is four-rank-ready, the computer system provides four chip-select signals, but the memory module **10** only uses two of the chip-select signals.

In certain embodiments, the circuit **40** comprises the SPD device **240** which reports the CAS latency (CL) to the memory controller of the computer system. The SPD device **240** of certain embodiments reports a CL which has one more cycle than does the actual operational CL of the memory array. In certain embodiments, data transfers between the memory controller and the memory module are registered for one additional clock cycle by the circuit **40**. The additional clock cycle of certain embodiments is added to the transfer time budget with an incremental overall CAS latency. This extra cycle of time in certain embodiments advantageously provides sufficient time budget to add a buffer which electrically isolates the ranks of memory devices **30** from the memory controller **20**. The buffer of certain embodiments comprises combinatorial logic, registers, and logic pipelines. In certain embodiments, the buffer adds a one-clock cycle time delay, which is equivalent to a registered DIMM, to accomplish the address decoding. The one-cycle time delay of certain such embodiments provides sufficient time for read and write data transfers to provide the functions of the data path multiplexer/demultiplexer. Thus, for example, a DDR2 400-MHz memory system in accordance with embodiments described herein has an overall CAS latency of four, and uses memory devices with a CAS latency of three. In still other embodiments, the SPD device **240** does not utilize this extra cycle of time.

Memory Density Multiplication

In certain embodiments, two memory devices having a memory density are used to simulate a single memory device having twice the memory density, and an additional

address signal bit is used to access the additional memory. Similarly, in certain embodiments, two ranks of memory devices having a memory density are used to simulate a single rank of memory devices having twice the memory density, and an additional address signal bit is used to access the additional memory. As used herein, such simulations of memory devices or ranks of memory devices are termed as "memory density multiplication," and the term "density transition bit" is used to refer to the additional address signal bit which is used to access the additional memory by selecting which rank of memory devices is enabled for a read or write transfer operation.

For example, for computer systems which are normally limited to using memory modules which have a single rank of 128 M×4-bit memory devices, certain embodiments described herein enable the computer system to utilize memory modules which have double the memory (e.g., two ranks of 128 M×4-bit memory devices). The circuit **40** of certain such embodiments provides the logic (e.g., command and address decoding logic) to double the number of chip selects, and the SPD device **240** reports a memory device density of 256 M×4-bit to the computer system.

In certain embodiments utilizing memory density multiplication embodiments, the memory module **10** can have various types of memory devices **30** (e.g., DDR1, DDR2, DDR3, and beyond). The circuit **40** of certain such embodiments utilizes implied translation logic equations having variations depending on whether the density transition bit is a row, column, or internal bank address bit. In addition, the translation logic equations of certain embodiments vary depending on the type of memory module **10** (e.g., UDIMM, RDIMM, FBDIMM, etc.). Furthermore, in certain embodiments, the translation logic equations vary depending on whether the implementation multiplies memory devices per rank or multiplies the number of ranks per memory module.

TABLE 3A

	128-Mb	256-Mb	512-Mb	1-Gb
Number of banks	4	4	4	4
Number of row address bits	12	13	13	14
Number of column address bits for "x 4" configuration	11	11	12	12
Number of column address bits for "x 8" configuration	10	10	11	11
Number of column address bits for "x 16" configuration	9	9	10	10

Table 3A provides the numbers of rows and columns for DDR-1 memory devices, as specified by JEDEC standard JESD79D, "Double Data Rate (DDR) SDRAM Specification," published February 2004, and incorporated in its entirety by reference herein.

As described by Table 3A, 512-Mb (128 M×4-bit) DRAM devices have 2^{13} rows and 2^{12} columns of memory locations, while 1-Gb (128 M×8-bit) DRAM devices have 2^{14} rows and 2^{11} columns of memory locations. Because of the differences in the number of rows and the number of columns for the two types of memory devices, complex address translation procedures and structures would typically be needed to fabricate a 1-GB (128 M×8-byte) memory module using sixteen 512-Mb (128 M×4-bit) DRAM devices.

Table 3B shows the device configurations as a function of memory density for DDR2 memory devices.

TABLE 3B

	Number of Rows	Number of Columns	Number of Internal Banks	Page Size (x4s or x8s)
256 Mb	13	11	4	1 KB
512 Mb	14	11	4	1 KB
1 Gb	14	11	8	1 KB
2 Gb	15	11	8	1 KB
4 Gb	16	11	8	1 KB

Table 4 lists the corresponding density transition bit for the density transitions between the DDR2 memory densities of Table 3B.

TABLE 4

Density Transition	Density Transition Bit
256 Mb to 512 Mb	A_{13}
512 Mb to 1 Gb	BA_2
1 Gb to 2 Gb	A_{14}
2 Gb to 4 Gb	A_{15}

Other certain embodiments described herein utilize a transition bit to provide a transition from pairs of physical 4-Gb memory devices to simulated 8-Gb memory devices.

In an example embodiment, the memory module comprises one or more pairs of 256-Mb memory devices, with each pair simulating a single 512-Mb memory device. The simulated 512-Mb memory device has four internal banks while each of the two 256-Mb memory devices has four internal banks, for a total of eight internal banks for the pair of 256-Mb memory devices. In certain embodiments, the additional row address bit is translated by the circuit **40** to the rank selection between each of the two 256-Mb memory devices of the pair. Although there are eight total internal banks in the rank-converted memory array, the computer system is only aware of four internal banks. When the memory controller activates a row for a selected bank, the circuit **40** activates the same row for the same bank, but it does so for the selected rank according to the logic state of the additional row address bit A_{13}.

In another example embodiment, the memory module comprises one or more pairs of 512-Mb memory devices, with each pair simulating a single 1-Gb memory device. The simulated 1-Gb memory device has eight internal banks while each of the two 512-Mb memory devices has four internal banks, for a total of eight internal banks for the pair of 512-Mb memory devices. In certain embodiments, the mapped BA_2 (bank 2) bit is used to select between the two ranks of 512-Mb memory devices to preserve the internal bank geometry expected by the memory controller of the computer system. The state of the BA_2 bit selects the upper or lower set of four banks, as well as the upper and lower 512-Mb rank.

In another example embodiment, the memory module comprises one or more pairs of 1-Gb memory devices, with each pair simulating a single 2-Gb memory device. Each of the two 1-Gb memory devices has eight internal banks for a total of sixteen internal banks, while the simulated 2-Gb memory device has eight internal banks. In certain embodiments, the additional row address bit translates to the rank selection between the two 1-Gb memory devices. Although there are sixteen total internal banks per pair of 1-Gb memory devices in the rank-converted memory array, the memory controller of the computer system is only aware of eight internal banks. When the memory controller activates a row of a selected bank, the circuit **40** activates the same

row for the same bank, but is does so for the selected rank according to the logic state of the additional row address bit A_{14}.

The circuit **40** of certain embodiments provides substantially all of the translation logic used for the decoding (e.g., command and address decoding). In certain such embodiments, there is a fully transparent operational conversion from the "system memory" density domain of the computer system to the "physical memory" density domain of the memory module **10**. In certain embodiments, the logic translation equations are programmed in the circuit **40** by hardware, while in certain other embodiments, the logic translation equations are programmed in the circuit **40** by software. Examples 1 and 2 provide exemplary sections of Verilog code compatible with certain embodiments described herein. As described more fully below, the code of Examples 1 and 2 includes logic to reduce potential problems due to "back-to-back adjacent read commands which cross memory device boundaries or "BBARX." Persons skilled in the art are able to provide additional logic translation equations compatible with embodiments described herein.

An exemplary section of Verilog code compatible with memory density multiplication from 512 Mb to 1 Gb using DDR2 memory devices with the BA_2 density transition bit is listed below in Example 2. The exemplary code of Example 2 corresponds to a circuit **40** which receives one chip-select signal from the computer system and which generates two chip-select signals.

Example 2

```
always @(posedge clk_in)
    begin
                rs0N_R <= rs0_in_N;    // cs0
                rasN_R <= ras_in_N;
                casN_R <= cas_in_N;
                weN_R <= we_in_N;
    end
// Gated Chip Selects
assign          pcs0a_1 = (~rs0_in_N & ~ras_in_N & ~cas_in_N)                          // ref,md reg set
                | (~rs0_in_N & ras_in_N & cas_in_N)                                    // ref exit, pwr dn
                | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & a10_in)               // pchg all
                | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & ~a10_in & ~ba2_in)    // pchg single bnk
                | (~rs0_in_N & ~ras_in_N & cas_in_N & we_in_N & ~ba2_in)               // activate
                | (~rs0_in_N & ras_in_N          & ~cas_in_N & ~ba2_in)                // xfr
                ;
assign          pcs0b_1 = (~rs0_in_N & ~ras_in_N & ~cas_in_N)                          // ref,md reg set
                | (~rs0_in_N & ras_in_N & cas_in_N)                                    // ref exit, pwr dn
                | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & a10_in)               // pchg all
                | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & ~a10_in & ba2_in)     // pchg single bnk
                | (~rs0_in_N & ~ras_in_N & cas_in_N & we_in_N & ba2_in)                // activate
                | (~rs0_in_N & ras_in_N          & ~cas_in_N & ba2_in)                 // xfr
                ;
//-------------------------------------
always @(posedge clk_in)
    begin
                a4_r <= a4_in ;
                a5_r <= a5_in ;
                a6_r <= a6_in ;
                a10_r <= a10_in ;
                ba0_r <= ba0_in ;
                ba1_r <= ba1_in ;
                ba2_r <= ba2_in ;
                q_mrs_cmd_cyc1 <= q_mrs_cmd ;
    end
////////////////////////////////////////////////////////////////////////
// determine the cas latency
////////////////////////////////////////////////////////////////////////
assign q_mrs_cmd_r = (!rasN_R & !casN_R & !weN_R)
                    & !rs0N_R
                & (!ba0_r & !ba1_r)
                ;       // md reg set cmd
    always @(posedge clk_in)
        if (~reset_N)       // lmr
                cl3 <= 1'b1 ;
        else if (q_mrs_cmd_cyc1)    // load mode reg cmd
      begin
                cl3 <= (~a6_r & a5_r & a4_r ) ;
      end
    always @(posedge clk_in)
        if (~reset_N)           // reset
                cl2 <= 1'b0 ;
        else if (q_mrs_cmd_cyc1)  // load mode reg cmd
      begin
                cl2 <= (~a6_r & a5_r & ~a4_r ) ;
      end
    always @(posedge clk_in)
        if (~reset_N)           // reset
                cl4 <= 1'b0 ;
        else if (q_mrs_cmd_cyc1)  // load mode reg cmd
      begin
```

-continued

```
                cl4 <= (a6_r & ~a5_r & ~a4_r ) ;
        end
  always @(posedge clk_in)
          if (~reset_N)             cl5 <= 1'b0 ;
          else if (q_mrs_cmd_cyc1)  // load mode reg cmd
        begin
                cl5 <= (a6_r & ~a5_r & a4_r ) ;
        end
assign          pre_cyc2_enfet = (wr_cmd_cyc1 & acs_cyc1 & cl3)     // wr brst cl3 preamble
                               ;
assign          pre_cyc3_enfet = (rd_cmd_cyc2 & cl3)                // rd brst cl3 preamble
                               | (wr_cmd_cyc2 & cl3)                // wr brst cl3 1st pair
                               | (wr_cmd_cyc2 & cl4)                // wr brst cl4 preamble
                               ;
assign          pre_cyc4_enfet = (wr_cmd_cyc3 & cl3)                // wr brst cl3 2nd pair
                               | (wr_cmd_cyc3 & cl4)                // wr brst cl4 1st pair
                               | (rd_cmd_cyc3 & cl3)                // rd brst cl3 1st pair
                               | (rd_cmd_cyc3 & cl4)                // rd brst cl4 preamble
                               ;
assign          pre_cyc5_enfet = (rd_cmd_cyc4 & cl3)                // rd brst cl3 2nd pair
                               | (wr_cmd_cyc4 & cl4)                // wr brst cl4 2nd pair
                               | (rd_cmd_cyc4 & cl4)                // rd brst cl4 1st pair
                               ;
// dq
assign          pre_dq_cyc = pre_cyc2_enfet
                   | pre_cyc3_enfet
                   | pre_cyc4_enfet
                   | pre_cyc5_enfet
                   ;
assign          pre_dq_ncyc = enfet_cyc2
                   | enfet_cyc3
                  | enfet_cyc4
                  | enfet_cyc5
                  ;
// dqs
assign          pre_dqsa_cyc = (pre_cyc2_enfet & ~ba2_r)
                  | (pre_cyc3_enfet & ~ba2_cyc2)
                  | (pre_cyc4_enfet & ~ba2_cyc3)
                  | (pre_cyc5_enfet & ~ba2_cyc4)
                  ;
assign          pre_dqsb_cyc = (pre_cyc2_enfet & ba2_r)
                  | (pre_cyc3_enfet & ba2_cyc2)
                  | (pre_cyc4_enfet & ba2_cyc3)
                  | (pre_cyc5_enfet & ba2_cyc4)
                  ;
assign          pre_dqsa_ncyc = (enfet_cyc2 & ~ba2_cyc2)
                  | (enfet_cyc3 & ~ba2_cyc3)
                  | (enfet_cyc4 & ~ba2_cyc4)
                  | (enfet_cyc5 & ~ba2_cyc5)
                  ;
assign          pre_dqsb_ncyc = (enfet_cyc2 & ba2_cyc2)
                  | (enfet_cyc3 & ba2_cyc3)
                  | (enfet_cyc4 & ba2_cyc4)
                  | (enfet_cyc5 & ba2_cyc5)
                  ;
always @(posedge clk_in)
        begin
                acs_cyc2 <= acs_cyc1 ;      // cs active
                ba2_cyc2 <= ba2_r ;
                ba2_cyc3 <= ba2_cyc2 ;
                ba2_cyc4 <= ba2_cyc3 ;
                ba2_cyc5 <= ba2_cyc4 ;
                rd_cmd_cyc2 <= rd_cmd_cyc1 & acs_cyc1;
                rd_cmd_cyc3 <= rd_cmd_cyc2 ;
                rd_cmd_cyc4 <= rd_cmd_cyc3 ;
                rd_cmd_cyc5 <= rd_cmd_cyc4 ;
                rd_cmd_cyc6 <= rd_cmd_cyc5 ;
                rd_cmd_cyc7 <= rd_cmd_cyc6 ;
                wr_cmd_cyc2 <= wr_cmd_cyc1 & acs_cyc1;
                wr_cmd_cyc3 <= wr_cmd_cyc2 ;
                wr_cmd_cyc4 <= wr_cmd_cyc3 ;
                wr_cmd_cyc5 <= wr_cmd_cyc4 ;
        end
 always @(negedge clk_in)
        begin
                dq_ncyc <= dq_cyc;
                dqs_ncyc_a <= dqs_cyc_a;
                dqs_ncyc_b <= dqs_cyc_b;
        end
```

-continued

```
// DQ FET enables
assign          enq_fet1 = dq_cyc | dq_ncyc          ;
assign          enq_fet2 = dq_cyc | dq_ncyc ;
assign          enq_fet3 = dq_cyc | dq_ncyc          ;
assign          enq_fet4 = dq_cyc | dq_ncyc ;
assign          enq_fet5 = dq_cyc | dq_ncyc ;
// DQS FET enables
assign          ens_fet1a = dqs_cyc_a | dqs_ncyc_a   ;
assign          ens_fet2a = dqs_cyc_a | dqs_ncyc_a   ;
assign          ens_fet3a = dqs_cyc_a | dqs_ncyc_a   ;
assign          ens_fet1b = dqs_cyc_b | dqs_ncyc_b   ;
assign          ens_fet2b = dqs_cyc_b | dqs_ncyc_b   ;
assign          ens_fet3b = dqs_cyc_b | dqs_ncyc_b   ;
```

Another exemplary section of Verilog code compatible with memory density multiplication from 256 Mb to 512 Mb using DDR2 memory devices and gated CAS signals with the row A_{13} density transition bit is listed below in Example 3. The exemplary code of Example 3 corresponds to a circuit **40** which receives one gated CAS signal from the computer system and which generates two gated CAS signals.

Example 3

```
// latched a13 flags cs0, banks 0-3
  always @(posedge clk_in)
    if (actv_cmd_R & ~rs0N_R & ~bnk1_R & ~bnk0_R )   // activate
    begin
                1_a13_00 <= a13_r ;
    end
  always @(posedge clk_in)
    if (actv_cmd_R & ~rs0N_R & ~bnk1_R & bnk0_R)     // activate
    begin
                1_a13_01 <= a13_r ;
    end
  always @(posedge clk_in)
    if (actv_cmd_R & ~rs0N_R & bnk1_R & ~bnk0_R)     // activate
    begin
                1_a13_10 <= a13_r ;
    end
  always @(posedge clk_in)
    if (actv_cmd_R & ~rs0N_R & bnk1_R & bnk0_R)      // activate
    begin
                1_a13_11 <= a13_r ;
    end
// gated cas
assign cas_i = ~(casN_R);
assign    cas0_o = ( ~rasN_R & cas_i)
                | ( rasN_R & ~1_a13_00 & ~bnk1_R & ~bnk0_R & cas_i)
                | ( rasN_R & ~1_a13_01 & ~bnk1_R & bnk0_R & cas_i)
                | ( rasN_R & ~1_a13_10 & bnk1_R & ~bnk0_R & cas_i)
                | ( rasN_R & ~1_a13_11 & bnk1_R & bnk0_R & cas_i)
                ;
assign    cas1_o = ( ~rasN_R & cas_i)
                | ( rasN_R & 1_a13_00          & ~bnk1_R & ~bnk0_R    & cas_i)
                | ( rasN_R & 1_a13_01           & ~bnk1_R & bnk0_R    & cas_i)
                | ( rasN_R & 1_a13_10           & bnk1_R & ~bnk0_R    & cas_i)
                | ( rasN_R & 1_a13_11           & bnk1_R & bnk0_R     & cas_i)
                ;
assign          pcas_0_N = ~cas0_o;
assign          pcas_1_N = ~cas1_o;
assign          rd0_o_R1 = rasN_R & cas0_o & weN_R & ~rs0N_R;   // rnk0 rd cmd cyc
assign          rd1_o_R1 = rasN_R & cas1_o & weN_R & ~rs0N_R;   // rnk1 rd cmd cyc
assign          wr0_o_R1 = rasN_R & cas0_o & ~weN_R & ~rs0N_R;  // rnk0 wr cmd cyc
assign          wr1_o_R1 = rasN_R & cas1_o & ~weN_R & ~rs0N_R ;  // rnk1 wr cmd cyc
      always @(posedge clk_in)
          begin
                rd0_o_R2 <= rd0_o_R1 ;
                rd0_o_R3 <= rd0_o_R2;
                rd0_o_R4 <= rd0_o_R3;
                rd0_o_R5 <= rd0_o_R4;
                rd1_o_R2 <= rd1_o_R1 ;
                rd1_o_R3 <= rd1_o_R2;
                rd1_o_R4 <= rd1_o_R3;
                rd1_o_R5 <= rd1_o_R4;
                wr0_o_R2 <= wr0_o_R1 ;
                wr0_o_R3 <= wr0_o_R2;
                wr0_o_R4 <= wr0_o_R3;
                wr1_o_R2 <= wr1_o_R1 ;
```

-continued

```
                wr1_o_R3 <= wr1_o_R2;
                wr1_o_R4 <= wr1_o_R3;
        end
    always @(posedge clk_in)
        begin
        if (
              (rd0_o_R2 & ~rd1_o_R4)                          // pre-am rd if no ped on rnk 1
            | rd0_o_R3                                        // 1st cyc of rd brst
            | rd0_o_R4                                        // 2nd cyc of rd brst
            | (rd0_o_R5 & ~rd1_o_R2 & ~rd1_o_R3)              // post-rd cyc if no ped on rnk 1
            | (wr0_o_R1)                                      // pre-am wr
            | wr0_o_R2 | wr0_o_R3                             // wr brst 1st & 2nd cyc
            | (wr0_o_R4)                                      // post-wr cyc (chgef9)
            | wr1_o_R1 | wr1_o_R2 | wr1_o_R3 | wr1_o_R4      // rank 1 (chgef9)
            )
                        en_fet_a <= 1'b1;                     // enable fet
        else
                        en_fet_a <= 1'b0;                     // disable fet
        end
always @(posedge clk_in)
        begin
        if (
                    (rd1_o_R2 & ~rd0_o_R4)
                  | rd1_o_R3
                  | rd1_o_R4
                  | (rd1_o_R5 & ~rd0_o_R2 & ~rd0_o_R3)
            | (wr1_o_R1)                                      // (chgef8)
            | wr1_o_R2 | wr1_o_R3
  | (wr1_o_R4)                                                // post-wr cyc      (chgef9)
  | wr0_o_R1 | wr0_o_R2 | wr0_o_R3 | wr0_o_R4                 // rank 0 (chgef9)
                    )
                        en_fet_b <= 1'b1;                     //
        else
                        en_fet_b <= 1'b0;
        end
```

In certain embodiments, the chipset memory controller of the computer system uses the inherent behavioral characteristics of the memory devices (e.g., DDR2 memory devices) to optimize throughput of the memory system. For example, for each internal bank in the memory array, a row (e.g., 1 KB page) is advantageously held activated for an extended period of time. The memory controller, by anticipating a high number of memory accesses or hits to a particular region of memory, can exercise this feature to advantageously eliminate time-consuming pre-charge cycles. In certain such embodiments in which two half-density memory devices are transparently substituted for a single full-density memory device (as reported by the SPD device **240** to the memory controller), the memory devices advantageously support the "open row" feature.

FIG. **10**A schematically illustrates an exemplary memory module **10** which doubles the rank density in accordance with certain embodiments described herein. The memory module **10** has a first memory capacity. The memory module **10** comprises a plurality of substantially identical memory devices **30** configured as a first rank **32***a* and a second rank **32***b*. In certain embodiments, the memory devices **30** of the first rank **32***a* are configured in pairs, and the memory devices **30** of the second rank **32***b* are also configured in pairs. In certain embodiments, the memory devices **30** of the first rank **32***a* are configured with their respective DQS pins tied together and the memory devices **30** of the second rank **32***b* are configured with their respective DQS pins tied together, as described more fully below. The memory module **10** further comprises a circuit **40** which receives a first set of address and command signals from a memory controller (not shown) of the computer system. The first set of address and command signals is compatible with a second memory capacity substantially equal to one-half of the first memory capacity. The circuit **40** translates the first set of address and command signals into a second set of address and command signals which is compatible with the first memory capacity of the memory module **10** and which is transmitted to the first rank **32***a* and the second rank **32***b*.

The first rank **32***a* of FIG. **10**A has 18 memory devices **30** and the second rank **32***b* of FIG. **10**A has 18 memory devices **30**. Other numbers of memory devices **30** in each of the ranks **32***a*, **32***b* are also compatible with embodiments described herein.

In the embodiment schematically illustrated by FIG. **10**A, the memory module **10** has a width of 8 bytes (or 64 bits) and each of the memory devices **30** of FIG. **10**A has a bit width of 4 bits. The 4-bit-wide ("×4") memory devices **30** of FIG. **10**A have one-half the width, but twice the depth of 8-bit-wide ("×8") memory devices. Thus, each pair of "×4" memory devices **30** has the same density as a single "×8" memory device, and pairs of "×4" memory devices **30** can be used instead of individual "×8" memory devices to provide the memory density of the memory module **10**. For example, a pair of 512-Mb 128 M×4-bit memory devices has the same memory density as a 1-Gb 128 M×8-bit memory device.

For two "×4" memory devices **30** to work in tandem to mimic a "×8" memory device, the relative DQS pins of the two memory devices **30** in certain embodiments are advantageously tied together, as described more fully below. In addition, to access the memory density of a high-density memory module **10** comprising pairs of "×4" memory devices **30**, an additional address line is used. While a high-density memory module comprising individual "×8" memory devices with the next-higher density would also utilize an additional address line, the additional address lines are different in the two memory module configurations.

For example, a 1-Gb 128 M×8-bit DDR-1 DRAM memory device uses row addresses A_{13}-A_0 and column addresses A_{11} and A_9-A_0. A pair of 512-Mb 128 M×4-bit DDR-1 DRAM memory devices uses row addresses A_{12}-A_0 and column addresses A_{12}, A_{11}, and A_9-A_0. In certain embodiments, a memory controller of a computer system utilizing a 1-GB 128 M×8 memory module **10** comprising pairs of the 512-Mb 128 M×4 memory devices **30** supplies the address and command signals including the extra row address (AD) to the memory module **10**. The circuit **40** receives the address and command signals from the memory controller and converts the extra row address (A_{13}) into an extra column address (A_{12}).

FIG. **10**B schematically illustrates an exemplary circuit **40** compatible with embodiments described herein. The circuit **40** is used for a memory module **10** comprising pairs of "×4" memory devices **30** which mimic individual "×8" memory devices. In certain embodiments, each pair has the respective DQS pins of the memory devices **30** tied together. In certain embodiments, as schematically illustrated by FIG. **10**B, the circuit **40** comprises a programmable-logic device (PLD) **42**, a first multiplexer **44** electrically coupled to the first rank **32***a* of memory devices **30**, and a second multiplexer **46** electrically coupled to the second rank **32***b* of memory devices **30**. In certain embodiments, the PLD **42** and the first and second multiplexers **44**, **46** are discrete elements, while in other certain embodiments, they are integrated within a single integrated circuit. Persons skilled in the art can select an appropriate PLD **42**, first multiplexer **44**, and second multiplexer **46** in accordance with embodiments described herein.

In the exemplary circuit **40** of FIG. **10**B, during a row access procedure (CAS is high), the first multiplexer **44** passes the A_{12} address through to the first rank **32**, the second multiplexer **46** passes the A_{12} address through to the second rank **34**, and the PLD **42** saves or latches the A_{13} address from the memory controller. In certain embodiments, a copy of the A_{13} address is saved by the PLD **42** for each of the internal banks (e.g., 4 internal banks) per memory device **30**. During a subsequent column access procedure (CAS is low), the first multiplexer **44** passes the previously-saved A_{13} address through to the first rank **32***a* as the A_{12} address and the second multiplexer **46** passes the previously-saved A_{13} address through to the second rank **32***b* as the A_{12} address. The first rank **32***a* and the second rank **32***b* thus interpret the previously-saved A_{13} row address as the current A_{12} column address. In this way, in certain embodiments, the circuit **40** translates the extra row address into an extra column address in accordance with certain embodiments described herein.

Thus, by allowing two lower-density memory devices to be used rather than one higher-density memory device, certain embodiments described herein provide the advantage of using lower-cost, lower-density memory devices to build "next-generation" higher-density memory modules. Certain embodiments advantageously allow the use of lower-cost readily-available 512-Mb DDR-2 SDRAM devices to replace more expensive 1-Gb DDR-2 SDRAM devices. Certain embodiments advantageously reduce the total cost of the resultant memory module.

FIG. **11**A schematically illustrates an exemplary memory module **10** which doubles number of ranks in accordance with certain embodiments described herein. The memory module **10** has a first plurality of memory locations with a first memory density. The memory module **10** comprises a plurality of substantially identical memory devices **30** configured as a first rank **32***a*, a second rank **32***b*, a third rank **32***c*, and a fourth rank **32***d*. The memory module **10** further comprises a circuit **40** which receives a first set of address and command signals from a memory controller (not shown). The first set of address and command signals is compatible with a second plurality of memory locations having a second memory density. The second memory density is substantially equal to one-half of the first memory density. The circuit **40** translates the first set of address and command signals into a second set of address and command signals which is compatible with the first plurality of memory locations of the memory module **10** and which is transmitted to the first rank **32***a*, the second rank **32***b*, the third rank **32***c*, and the fourth rank **32***d*.

Each rank **32***a*, **32***b*, **32***c*, **32***d* of FIG. **11**A has 9 memory devices **30**. Other numbers of memory devices **30** in each of the ranks **32***a*, **32***b*, **32***c*, **32***d* are also compatible with embodiments described herein.

In the embodiment schematically illustrated by FIG. **11**A, the memory module **10** has a width of 8 bytes (or 64 bits) and each of the memory devices **30** of FIG. **11**A has a bit width of 8 bits. Because the memory module **10** has twice the number of 8-bit-wide ("×8") memory devices **30** as does a standard 8-byte-wide memory module, the memory module **10** has twice the density as does a standard 8-byte-wide memory module. For example, a 1-GB 128 M×8-byte memory module with 36 512-Mb 128 M×8-bit memory devices (arranged in four ranks) has twice the memory density as a 512-Mb 128 M×8-byte memory module with 18 512-Mb 128 M×8-bit memory devices (arranged in two ranks).

To access the additional memory density of the high-density memory module **10**, the two chip-select signals (CS_0, CS_1) are used with other address and command signals to gate a set of four gated CAS signals. For example, to access the additional ranks of four-rank 1-GB 128 M×8-byte DDR-1 DRAM memory module, the CS_0 and CS_1 signals along with the other address and command signals are used to gate the CAS signal appropriately, as schematically illustrated by FIG. **11**A. FIG. **11**B schematically illustrates an exemplary circuit **40** compatible with embodiments described herein. In certain embodiments, the circuit **40** comprises a programmable-logic device (PLD) **42** and four "OR" logic elements **52**, **54**, **56**, **58** electrically coupled to corresponding ranks **32***a*, **32***b*, **32***c*, **32***d* of memory devices **30**.

In certain embodiments, the PLD **42** comprises an ASIC, an FPGA, a custom-designed semiconductor device, or a CPLD. In certain embodiments, the PLD **42** and the four "OR" logic elements **52**, **54**, **56**, **58** are discrete elements, while in other certain embodiments, they are integrated within a single integrated circuit. Persons skilled in the art can select an appropriate PLD **42** and appropriate "OR" logic elements **52**, **54**, **56**, **58** in accordance with embodiments described herein.

In the embodiment schematically illustrated by FIG. **11**B, the PLD **42** transmits each of the four "enabled CAS" ($ENCAS_0a$, $ENCAS_0b$, $ENCAS_1a$, $ENCAS_1b$) signals to a corresponding one of the "OR" logic elements **52**, **54**, **56**, **58**. The CAS signal is also transmitted to each of the four "OR" logic elements **52**, **54**, **56**, **58**. The CAS signal and the "enabled CAS" signals are "low" true signals. By selectively activating each of the four "enabled CAS" signals which are inputted into the four "OR" logic elements **52**, **54**, **56**, **58**, the PLD **42** is able to select which of the four ranks **32***a*, **32***b*, **32***c*, **32***d* is active.

In certain embodiments, the PLD **42** uses sequential and combinatorial logic procedures to produce the gated CAS

signals which are each transmitted to a corresponding one of the four ranks **32***a*, **32***b*, **32***c*, **32***d*. In certain other embodiments, the PLD **42** instead uses sequential and combinatorial logic procedures to produce four gated chip-select signals (e.g., CS_0a, CS_0b, CS_1a, and CS_1b) which are each transmitted to a corresponding one of the four ranks **32***a*, **32***b*, **32***c*, **32***d*.

Tied Data Strobe Signal Pins

For proper operation, the computer system advantageously recognizes a 1-GB memory module comprising 256-Mb memory devices with 64 M×4-bit configuration as a 1-GB memory module having 512-Mb memory devices with 64 M×8-bit configuration (e.g., as a 1-GB memory module with 128 M×8-byte configuration). This advantageous result is desirably achieved in certain embodiments by electrically connecting together two output signal pins (e.g., DQS or data strobe pins) of the two 256-Mb memory devices such that both output signal pins are concurrently active when the two memory devices are concurrently enabled. The DQS or data strobe is a bi-directional signal that is used during both read cycles and write cycles to validate or latch data. As used herein, the terms "tying together" or "tied together" refer to a configuration in which corresponding pins (e.g., DQS pins) of two memory devices are electrically connected together and are concurrently active when the two memory devices are concurrently enabled (e.g., by a common chip-select or CS signal). Such a configuration is different from standard memory module configurations in which the output signal pins (e.g., DQS pins) of two memory devices are electrically coupled to the same source, but these pins are not concurrently active since the memory devices are not concurrently enabled. However, a general guideline of memory module design warns against tying together two output signal pins in this way.

FIGS. **12** and **13** schematically illustrate a problem which may arise from tying together two output signal pins. FIG. **12** schematically illustrates an exemplary memory module **305** in which a first DQS pin **312** of a first memory device **310** is electrically connected to a second DQS pin **322** of a second memory device **320**. The two DQS pins **312**, **322** are both electrically connected to a memory controller **330**.

FIG. **13** is an exemplary timing diagram of the voltages applied to the two DQS pins **312**, **322** due to non-simultaneous switching. As illustrated by FIG. **13**, at time t_1, both the first DQS pin **312** and the second DQS pin **322** are high, so no current flows between them. Similarly, at time t_4, both the first DQS pin **312** and the second DQS pin **322** are low, so no current flows between them. However, for times between approximately t_2 and approximately t_3, the first DQS pin **312** is low while the second DQS pin **322** is high. Under such conditions, a current will flow between the two DQS pins **312**, **322**. This condition in which one DQS pin is low while the other DQS pin is high can occur for fractions of a second (e.g., 0.8 nanoseconds) during the dynamic random-access memory (DRAM) read cycle. During such conditions, the current flowing between the two DQS pins **312**, **322** can be substantial, resulting in heating of the memory devices **310**, **320**, and contributing to the degradation of reliability and eventual failure of these memory devices.

A second problem may also arise from tying together two output signal pins. FIG. **14** schematically illustrates another exemplary memory module **305** in which a first DQS pin **312** of a first memory device **310** is electrically connected to a second DQS pin **322** of a second memory device **320**. The two DQS pins **312**, **322** of FIG. **14** are both electrically connected to a memory controller (not shown). The DQ (data input/output) pin **314** of the first memory device **310** and the corresponding DQ pin **324** of the second memory device **320** are each electrically connected to the memory controller by the DQ bus (not shown). Typically, each memory device **310**, **320** will have a plurality of DQ pins (e.g., eight DQ pins per memory device), but for simplicity, FIG. **14** only shows one DQ pin for each memory device **310**, **320**.

Each of the memory devices **310**, **320** of FIG. **14** utilizes a respective on-die termination or "ODT" circuit **332**, **334** which has termination resistors (e.g., 75 ohms) internal to the memory devices **310**, **320** to provide signal termination. Each memory device **310**, **320** has a corresponding ODT signal pin **362**, **364** which is electrically connected to the memory controller via an ODT bus **340**. The ODT signal pin **362** of the first memory device **310** receives a signal from the ODT bus **340** and provides the signal to the ODT circuit **332** of the first memory device **310**. The ODT circuit **332** responds to the signal by selectively enabling or disabling the internal termination resistors **352**, **356** of the first memory device **310**. This behavior is shown schematically in FIG. **14** by the switches **342**, **344** which are either closed (dash-dot line) or opened (solid line). The ODT signal pin **364** of the second memory device **320** receives a signal from the ODT bus **340** and provides the signal to the ODT circuit **334** of the second memory device **320**. The ODT circuit **334** responds to the signal by selectively enabling or disabling the internal termination resistors **354**, **358** of the second memory device **320**. This behavior is shown schematically in FIG. **14** by the switches **346**, **348** which are either closed (dash-dot line) or opened (solid line). The switches **342**, **344**, **346**, **348** of FIG. **14** are schematic representations of the operation of the ODT circuits **332**, **334**, and do not signify that the ODT circuits **332**, **334** necessarily include mechanical switches.

Examples of memory devices **310**, **320** which include such ODT circuits **332**, **334** include, but are not limited to, DDR2 memory devices. Such memory devices are configured to selectively enable or disable the termination of the memory device in this way in response to signals applied to the ODT signal pin of the memory device. For example, when the ODT signal pin **362** of the first memory device **310** is pulled high, the termination resistors **352**, **356** of the first memory device **310** are enabled. When the ODT signal pin **362** of the first memory device **310** is pulled low (e.g., grounded), the termination resistors **352**, **356** of the first memory device **310** are disabled. By selectively disabling the termination resistors of an active memory device, while leaving the termination resistors of inactive memory devices enabled, such configurations advantageously preserve signal strength on the active memory device while continuing to eliminate signal reflections at the bus-die interface of the inactive memory devices.

In certain configurations, as schematically illustrated by FIG. **14**, the DQS pins **312**, **322** of each memory device **310**, **320** are selectively connected to a voltage VTT through a corresponding termination resistor **352**, **354** internal to the corresponding memory device **310**, **320**. Similarly, in certain configurations, as schematically illustrated by FIG. **14**, the DQ pins **314**, **324** are selectively connected to a voltage VTT through a corresponding termination resistor **356**, **358** internal to the corresponding memory device **310**, **320**. In certain configurations, rather than being connected to a voltage VTT, the DQ pins **314**, **324** and/or the DQS pins **312**, **322** are selectively connected to ground through the corresponding termination resistors **352**, **354**, **356**, **358**. The resistances of the internal termination resistors **352**, **354**, **356**, **358** are

selected to clamp the voltages so as to reduce the signal reflections from the corresponding pins. In the configuration schematically illustrated by FIG. **14**, each internal termination resistor **352**, **354**, **356**, **358** has a resistance of approximately 75 ohms.

When connecting the first memory device **310** and, the second memory device **320** together to form a double word width, both the first memory device **310** and the second memory device **320** are enabled at the same time (e.g., by a common CS signal). Connecting the first memory device **310** and the second memory device **320** by tying the DQS pins **312**, **322** together, as shown in FIG. **14**, results in a reduced effective termination resistance for the DQS pins **312**, **322**. For example, for the exemplary configuration of FIG. **14**, the effective termination resistance for the DQS pins **312**, **322** is approximately 37.5 ohms, which is one-half the desired ODT resistance (for 75-ohm internal termination resistors) to reduce signal reflections since the internal termination resistors **352**, **354** of the two memory devices **310**, **320** are connected in parallel. This reduction in the termination resistance can result in signal reflections causing the memory device to malfunction.

FIG. **15** schematically illustrates an exemplary memory module **400** in accordance with certain embodiments described herein. The memory module **400** comprises a first memory device **410** having a first data strobe (DQS) pin **412** and a second memory device **420** having a second data strobe (DQS) pin **422**. The memory module **400** further comprises a first resistor **430** electrically coupled to the first DQS pin **412**. The memory module **400** further comprises a second resistor **440** electrically coupled to the second DQS pin **422** and to the first resistor **430**. The first DQS pin **412** is electrically coupled to the second DQS pin **422** through the first resistor **430** and through the second resistor **440**.

In certain embodiments, the memory module **400** is a 1-GB unbuffered Double Data Rate (DDR) Synchronous Dynamic RAM (SDRAM) high-density dual in-line memory module (DIMM). FIGS. **16**A and **16**B schematically illustrate a first side **462** and a second side **464**, respectively, of such a memory module **400** with eighteen 64 M×4-bit, DDR-1 SDRAM FBGA memory devices on each side of a 184-pin glass-epoxy printed circuit board (PCB) **460**. In certain embodiments, the memory module **400** further comprises a phase-lock-loop (PLL) clock driver **470**, an EEPROM for serial-presence detect (SPD) data **480**, and decoupling capacitors (not shown) mounted on the PCB in parallel to suppress switching noise on VDD and VDDQ power supply for DDR-1 SDRAM. By using synchronous design, such memory modules **400** allow precise control of data transfer between the memory module **400** and the system controller. Data transfer can take place on both edges of the DQS signal at various operating frequencies and programming latencies. Therefore, certain such memory modules **400** are suitable for a variety of high-performance system applications.

In certain embodiments, the memory module **400** comprises a plurality of memory devices configured in pairs, each pair having a first memory device **410** and a second memory device **420**. For example, in certain embodiments, a 128 M×72-bit DDR SDRAM high-density memory module **400** comprises thirty-six 64 M×4-bit DDR-1 SDRAM integrated circuits in FBGA packages configured in eighteen pairs. The first memory device **410** of each pair has the first DQS pin **412** electrically coupled to the second DQS pin **422** of the second memory device **420** of the pair. In addition, the first DQS pin **412** and the second DQS pin **422** are concurrently active when the first memory device **410** and the second memory device **420** are concurrently enabled.

In certain embodiments, the first resistor **430** and the second resistor **440** each has a resistance advantageously selected to reduce the current flow between the first DQS pin **412** and the second DQS pin **422** while allowing signals to propagate between the memory controller and the DQS pins **412**, **422**. In certain embodiments, each of the first resistor **430** and the second resistor **440** has a resistance in a range between approximately 5 ohms and approximately 50 ohms. For example, in certain embodiments, each of the first resistor **430** and the second resistor **440** has a resistance of approximately 22 ohms. Other resistance values for the first resistor **430** and the second resistor **440** are also compatible with embodiments described herein. In certain embodiments, the first resistor **430** comprises a single resistor, while in other embodiments, the first resistor **430** comprises a plurality of resistors electrically coupled together in series and/or in parallel. Similarly, in certain embodiments, the second resistor **440** comprises a single resistor, while in other embodiments, the second resistor **440** comprises a plurality of resistors electrically coupled together in series and/or in parallel.

FIGS. **17**A and **17**B schematically illustrate an exemplary embodiment of a memory module **400** in which the first resistor **430** and the second resistor **440** are used to reduce the current flow between the first DQS pin **412** and the second DQS pin **422**. As schematically illustrated by FIG. **17**A, the memory module **400** is part of a computer system **500** having a memory controller **510**. The first resistor **430** has a resistance of approximately 22 ohms and the second resistor **440** has a resistance of approximately 22 ohms. The first resistor **430** and the second resistor **440** are electrically coupled in parallel to the memory controller **510** through a signal line **520** having a resistance of approximately 25 ohms. The first resistor **430** and the second resistor **440** are also electrically coupled in parallel to a source of a fixed termination voltage (identified by VTT in FIGS. **17**A and **17**B) by a signal line **540** having a resistance of approximately 47 ohms. Such an embodiment can advantageously be used to allow two memory devices having lower bit widths (e.g., 4-bit) to behave as a single virtual memory device having a higher bit width (e.g., 8-bit).

FIG. **17**B schematically illustrates exemplary current-limiting resistors **430**, **440** in conjunction with the impedances of the memory devices **410**, **420**. During an exemplary portion of a data read operation, the memory controller **510** is in a high-impedance condition, the first memory device **410** drives the first DQS pin **412** high (e.g., 2.7 volts), and the second memory device **420** drives the second DQS pin **422** low (e.g., 0 volts). The amount of time for which this condition occurs is approximated by the time between t_2 and t_3 of FIG. **13**, which in certain embodiments is approximately twice the tDQSQ (data strobe edge to output data edge skew time, e.g., approximately 0.8 nanoseconds). At least a portion of this time in certain embodiments is caused by simultaneous switching output (SSO) effects.

In certain embodiments, as schematically illustrated by FIG. **17**B, the DQS driver of the first memory device **410** has a driver impedance R_1 of approximately 17 ohms, and the DQS driver of the second memory device **420** has a driver impedance R_4 of approximately 17 ohms. Because the upper network of the first memory device **410** and the first resistor **430** (with a resistance R_2 of approximately 22 ohms) is approximately equal to the lower network of the second memory device **420** and the second resistor **440** (with a resistance R_3 of approximately 22 ohms), the voltage at the

midpoint is approximately 0.5*(2.7−0)=1.35 volts, which equals VTT, such that the current flow across the 47-ohm resistor of FIG. **17**B is approximately zero.

The voltage at the second DQS pin **422** in FIG. **17**B is given by $V_{DQS2}=2.7*R_4/(R_1+R_2+R_3+R_4)=0.59$ volts and the current flowing through the second DQS pin **422** is given by $I_{DQS2}=0.59/R_4=34$ milliamps. The power dissipation in the DQS driver of the second memory device **420** is thus $P_{DQS2}=34$ mA*0.59 V=20 milliwatts. In contrast, without the first resistor **430** and the second resistor **440**, only the 17-ohm impedances of the two memory devices **410**, **420** would limit the current flow between the two DQS pins **412**, **422**, and the power dissipation in the DQS driver of the second memory device **420** would be approximately 107 milliwatts. Therefore, the first resistor **430** and the second resistor **440** of FIGS. **17**A and **17**B advantageously limit the current flowing between the two memory devices during the time that the DQS pin of one memory device is driven high and the DQS pin of the other memory device is driven low.

In certain embodiments in which there is overshoot or undershoot of the voltages, the amount of current flow can be higher than those expected for nominal voltage values. Therefore, in certain embodiments, the resistances of the first resistor **430** and the second resistor **440** are advantageously selected to account for such overshoot/undershoot of voltages.

For certain such embodiments in which the voltage at the second DQS pin **422** is $V_{DQS2}=0.59$ volts and the duration of the overdrive condition is approximately 0.8 nanoseconds at maximum, the total surge is approximately 0.59 V*1.2 ns=0.3 V-ns. For comparison, the JEDEC standard for overshoot/undershoot is 2.4 V-ns, so certain embodiments described herein advantageously keep the total surge within predetermined standards (e.g., JEDEC standards).

FIG. **18** schematically illustrates another exemplary memory module **600** compatible with certain embodiments described herein. The memory module **600** comprises a termination bus **605**. The memory module **600** further comprises a first memory device **610** having a first data strobe pin **612**, a first termination signal pin **614** electrically coupled to the termination bus **605**, a first termination circuit **616**, and at least one data pin **618**. The first termination circuit **616** selectively electrically terminating the first data strobe pin **612** and the first data pin **618** in response to a first signal received by the first termination signal pin **614** from the termination bus **605**. The memory module **600** further comprises a second memory device **620** having a second data strobe pin **622** electrically coupled to the first data strobe pin **612**, a second termination signal pin **624**, a second termination circuit **626**, and at least one data pin **628**. The second termination signal pin **624** is electrically coupled to a voltage, wherein the second termination circuit **626** is responsive to the voltage by not terminating the second data strobe pin **622** or the second data pin **628**. The memory module **600** further comprises at least one termination assembly **630** having a third termination signal pin **634**, a third termination circuit **636**, and at least one termination pin **638** electrically coupled to the data pin **628** of the second memory device **620**. The third termination signal pin **634** is electrically coupled to the termination bus **605**. The third termination circuit **636** selectively electrically terminates the data pin **628** of the second memory device **620** through the termination pin **638** in response to a second signal received by the third termination signal pin **634** from the termination bus **605**.

FIG. **19** schematically illustrates a particular embodiment of the memory module **600** schematically illustrated by FIG. **18**. The memory module **600** comprises an on-die termination (ODT) bus **605**. The memory module **600** comprises a first memory device **610** having a first data strobe (DQS) pin **612**, a first ODT signal pin **614** electrically coupled to the ODT bus **605**, a first ODT circuit **616**, and at least one data (DQ) pin **618**. The first ODT circuit **616** selectively electrically terminates the first DQS pin **612** and the DQ pin **618** of the first memory device **610** in response to an ODT signal received by the first ODT signal pin **614** from the ODT bus **605**. This behavior of the first ODT circuit **616** is schematically illustrated in FIG. **14** by the switches **672**, **676** which are selectively closed (dash-dot line) or opened (solid line).

The memory module **600** further comprises a second memory device **620** having a second DQS pin **622** electrically coupled to the first DQS pin **612**, a second ODT signal pin **624**, a second ODT circuit **626**, and at least one DQ pin **628**. The first DQS pin **612** and the second DQS pin **622** are concurrently active when the first memory device **610** and the second memory device **620** are concurrently enabled. The second ODT signal pin **624** is electrically coupled to a voltage (e.g., ground), wherein the second ODT circuit **626** is responsive to the voltage by not terminating the second DQS pin **622** or the second DQ pin **624**. This behavior of the second ODT circuit **626** is schematically illustrated in FIG. **14** by the switches **674**, **678** which are opened.

The memory module **600** further comprises at least one termination assembly **630** having a third ODT signal pin **634** electrically coupled to the ODT bus **605**, a third ODT circuit **636**, and at least one termination pin **638** electrically coupled to the DQ pin **628** of the second memory device **620**. The third ODT circuit **636** selectively electrically terminates the DQ pin **628** of the second memory device **620** through the termination pin **638** in response to an ODT signal received by the third ODT signal pin **634** from the ODT bus **605**. This behavior of the third ODT circuit **636** is schematically illustrated in FIG. **19** by the switch **680** which is either closed (dash-dot line) or opened (solid line).

In certain embodiments, the termination assembly **630** comprises discrete electrical components which are surface-mounted or embedded on the printed-circuit board of the memory module **600**. In certain other embodiments, the termination assembly **630** comprises an integrated circuit mounted on the printed-circuit board of the memory module **600**. Persons skilled in the art can provide a termination assembly **630** in accordance with embodiments described herein.

Certain embodiments of the memory module **600** schematically illustrated by FIG. **19** advantageously avoid the problem schematically illustrated by FIG. **12** of electrically connecting the internal termination resistances of the DQS pins of the two memory devices in parallel. As described above in relation to FIG. **14**, FIGS. **18** and **19** only show one DQ pin for each memory device for simplicity. Other embodiments have a plurality of DQ pins for each memory device. In certain embodiments, each of the first ODT circuit **616**, the second ODT circuit **626**, and the third ODT circuit **636** are responsive to a high voltage or signal level by enabling the corresponding termination resistors and are responsive to a low voltage or signal level (e.g., ground) by disabling the corresponding termination resistors. In other embodiments, each of the first ODT circuit **616**, the second ODT circuit **626**, and the third ODT circuit **636** are responsive to a high voltage or signal level by disabling the corresponding termination resistors and are responsive to a low voltage or signal level (e.g., ground) by enabling the corresponding termination resistors. Furthermore, the switches **672**, **674**, **676**, **678**, **680** of FIG. **18** are schematic

representations of the enabling and disabling operation of the ODT circuits **616**, **626**, **636** and do not signify that the ODT circuits **616**, **626**, **636** necessarily include mechanical switches.

The first ODT signal pin **614** of the first memory device **610** receives an ODT signal from the ODT bus **605**. In response to this ODT signal, the first ODT circuit **616** selectively enables or disables the termination resistance for both the first DQS pin **612** and the DQ pin **618** of the first memory device **610**. The second ODT signal pin **624** of the second memory device **620** is tied (e.g., directly hard-wired) to the voltage (e.g., ground), thereby disabling the internal termination resistors **654**, **658** on the second DQS pin **622** and the second DQ pin **628**, respectively, of the second memory device **620** (schematically shown by open switches **674**, **678** in FIG. **19**). The second DQS pin **622** is electrically coupled to the first DQS pin **612**, so the termination resistance for both the first DQS pin **612** and the second DQS pin **622** is provided by the termination resistor **652** internal to the first memory device **510**.

The termination resistor **656** of the DQ pin **618** of the first memory device **610** is enabled or disabled by the ODT signal received by the first ODT signal pin **614** of the first memory device **610** from the ODT bus **605**. The termination resistance of the DQ pin **628** of the second memory device **620** is enabled or disabled by the ODT signal received by the third ODT signal pin **634** of the termination assembly **630** which is external to the second memory device **620**. Thus, in certain embodiments, the first ODT signal pin **614** and the third ODT signal pin **634** receive the same ODT signal from the ODT bus **605**, and the termination resistances for both the first memory device **610** and the second memory device **620** are selectively enabled or disabled in response thereto when these memory devices are concurrently enabled. In this way, certain embodiments of the memory module **600** schematically illustrated by FIG. **19** provides external or off-chip termination of the second memory device **620**.

Certain embodiments of the memory module **600** schematically illustrated by FIG. **19** advantageously allow the use of two lower-cost readily-available 512-Mb DDR-2 SDRAM devices to provide the capabilities of a more expensive 1-GB DDR-2 SDRAM device. Certain such embodiments advantageously reduce the total cost of the resultant memory module **600**.

Certain embodiments described herein advantageously increase the memory capacity or memory density per memory slot or socket on the system board of the computer system. Certain embodiments advantageously allow for higher memory capacity in systems with limited memory slots. Certain embodiments advantageously allow for flexibility in system board design by allowing the memory module **10** to be used with computer systems designed for different numbers of ranks (e.g., either with computer systems designed for two-rank memory modules or with computer systems designed for four-rank memory modules). Certain embodiments advantageously provide lower costs of board designs.

In certain embodiments, the memory density of a memory module is advantageously doubled by providing twice as many memory devices as would otherwise be provided. For example, pairs of lower-density memory devices can be substituted for individual higher-density memory devices to reduce costs or to increase performance. As another example, twice the number of memory devices can be used to produce a higher-density memory configuration of the memory module. Each of these examples can be limited by the number of chip select signals which are available from the memory controller or by the size of the memory devices. Certain embodiments described herein advantageously provide a logic mechanism to overcome such limitations.

Various embodiments of the present invention have been described above. Although this invention has been described with reference to these specific embodiments, the descriptions are intended to be illustrative of the invention and are not intended to be limiting. Various modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention.

We claim:

1. A memory module operable in a computer system to communicate data with a memory controller of the computer system at a specified data rate via a N-bit wide data bus in response to memory commands received from the memory controller, the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first burst of N-bit wide data signals and a first burst of data strobes and the second memory command to cause the memory module to receive or output a second burst of N-bit wide data signals and a second burst of data strobes, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, wherein the plurality of N-bit wide ranks include a first rank configured to receive or output the first burst of N-bit wide data signals and the first burst of data strobes at the specified data rate in response to the first memory command, and a second rank configured to receive or output the second burst of N-bit wide data signals and the second burst of data strobes at the specified data rate in response to the second memory command;

circuitry coupled between the plurality of N-bit wide ranks and the N-bit wide data bus; and

logic coupled to the circuitry and configured to respond to the first memory command by providing first control signals to the circuitry and to subsequently respond to the second memory command by providing second control signals to the circuitry, wherein the circuitry is configured to enable data transfers through the circuitry in response to the first control signals and subsequently in response to the second control signals, wherein respective N-bit wide data signals of the first burst of N-bit wide data signals and respective data strobes of the first burst of data strobes are transferred at the specified data rate between the first rank and the N-bit wide data bus through the circuitry, and wherein respective N-bit wide data signals of the second burst of N-bit wide data signals and respective data strobes of the second burst of data strobes are transferred at the specified data rate between the second rank and the N-bit wide data bus through the circuitry;

wherein the data transfers through the circuitry are registered data transfers enabled in accordance with an overall CAS latency of the memory module, and the circuitry is configured to add a predetermined amount of time delay for each registered data transfer through the circuitry so that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the plurality of memory integrated circuits.

2. The memory module of claim 1, wherein each of the plurality memory integrated circuits has a corresponding load, and wherein the circuitry is configured to isolate the loads of the plurality of memory integrated circuits from the memory controller.

3. The memory module of claim 1, wherein the logic is coupled to the printed circuit board and is further configured to receive from the memory controller a first set of input address and control signals associated with the first memory command and to respond to the first memory command by outputting a first set of registered address and control signals, and wherein the logic is further configured to subsequently receive from the memory controller a second set of input address and control signals associated with the second memory command and to respond to the second memory command by outputting a second set of registered address and control signals, the first set of input address and control signals including a first set of input chip select signals corresponding to respective ranks of the plurality of ranks and the second set of input address and control signals including a second set of input chip select signals corresponding to respective ranks of the plurality of ranks, the first set of registered address and control signals including a first plurality of registered chip select signals corresponding to respective ones of the first plurality of input chip select signals, the second set of registered address and control signals including a second plurality of registered chip select signals corresponding to respective ones of the second plurality of input chip select signals. the first set of registered chip select signals including a first registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value, the second set of registered chip select signals including a second registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value, and wherein the logic is configured to output the first registered chip select signal to the first rank and to output the second registered chip select signal to the second rank.

4. The memory module of claim 1, further comprising an SPD device that reports the overall CAS latency of the memory module to the memory controller.

5. The memory module of claim 1, wherein the memory module is configured to receive from the memory controller an on-die-termination (ODT) signal, wherein each of the plurality of memory integrated circuits includes an ODT circuit, the memory module further comprising a termination circuit external to any of the plurality of memory integrated circuits, wherein the termination circuit is configured to receive the ODT signal and is coupled to the ODT circuit of at least one of the plurality of memory integrated circuits, wherein the termination circuit is configured to provide external termination for the at least one of the plurality of memory integrated circuits in response to the ODT signal, and wherein the ODT circuit of the at least one of the plurality of memory integrated circuits is disabled.

6. The memory module of claim 1, wherein the circuitry includes logic pipelines configured to enable the data transfers through the circuitry in response to the first control signals and subsequently in response to the second control signals.

7. The memory module of claim 1, wherein the logic is further configured to determine the overall CAS latency of the memory module.

8. The memory module of claim 1, wherein N is 64 or 72.

9. The memory module of claim 1, wherein each rank of the plurality of ranks is 72-bits wide, wherein each rank of the plurality of N-bit wide ranks includes 18 4-bit wide memory integrated circuits configured in 9 pairs, wherein a first pair of memory integrated circuits in the first rank is configured to communicate a respective byte of the first burst of N-bit wide data signals in each time interval of a first plurality of time intervals, and wherein a second pair of memory integrated circuits in the second rank is configured to communicate a respective byte of the second burst of N-bit wide data signals in each time interval of a second plurality of time intervals.

10. The memory module of claim 9, wherein the first pair of memory integrated circuits are configured to simulate an 8-bit wide memory device, and the second pair of memory integrated circuits are configured to simulate another 8-bit wide memory device.

11. The memory module of claim 9, further comprising an SPD device programmed with data to characterize each pair of memory integrated circuits as a virtual 8-bit wide memory device.

12. The memory module of claim 1, wherein the respective N-bit wide data signals of the first burst of N-bit wide data signals and the respective data strobes of the first burst of data strobes are transferred through the circuitry during respective time intervals of a first plurality of time intervals, and wherein the respective N-bit wide data signals of the second burst of N-bit wide data signals and the respective data strobes of the second burst of data strobes are transferred through the circuitry during respective time intervals of a second plurality of time intervals.

13. The memory module of claim 1, further comprising a phase locked loop clock driver configured to output a clock signal in response to one or more signals received from the memory controller, wherein the predetermined amount of time delay is at least one clock cycle time delay.

14. The memory module of claim 13, wherein the memory integrated circuits are dynamic random access memory integrated circuits configured to operate synchronously with the clock signal, wherein each memory integrated circuit in the first rank is configured receive or output a respective set of bits of the first burst of N-bit wide data signals on both edges of each of a respective set of data strobes of the first burst of data strobes, and wherein each memory integrated circuit in the second rank is configured receive or output a respective set of bits of the second burst of N-bit wide data signals on both edges of each of a respective set of data strobes of the second burst of data strobes.

15. A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

logic coupled to the printed circuit board and configured to receive a first set of input address and control signals associated with a first read or write memory command and to output a first set of registered address and control signals in response to the first set of input address and control signals, the first set of input address and control signals including a first plurality of input chip select signals, the first set of registered address and control signals including a first plurality of registered chip select signals corresponding to respective ones of the first plurality of input chip select signals, the first plurality of registered chip select signals including a

first registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value;

memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, wherein the plurality of N-bit wide ranks are configured to receive respective ones of the first plurality of registered chip select signals, wherein a first N-bit wide rank in the plurality of N-bit wide ranks receiving the first registered chip select signal having the active signal value is configured to receive or output a first burst of N-bit wide data signals and a first burst of data strobes associated with the first read or write command;

circuitry coupled between data and strobe signal lines in the N-bit wide memory bus and corresponding data and strobe pins of memory devices in each of the plurality of N-bit wide ranks; and

wherein the logic is further configured to, in response to the first read or write memory command, output first control signals to the circuitry, and wherein the circuitry is configured to enable data transfers between the first rank and the memory bus through the circuitry in response to the first control signals so that respective N-bit wide data signals of the first burst of N-bit wide data signals and respective data strobes of the first burst of data strobes are transferred through the circuitry in accordance with an overall CAS latency of the memory module; and

wherein the data transfers between the first rank and the memory bus through the circuitry are registered data transfers and the circuitry is configured to add a predetermined amount of time delay for each registered data transfer through the circuitry such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.

16. The memory module of claim **15**, wherein each of the memory devices has a corresponding load, and the circuitry is configured to isolate the loads of the memory devices from the memory bus.

17. The memory module of claim **15**, wherein the first burst of N-bit wide data signals includes a set of consecutively transmitted data bits for each data signal line in the memory bus, and wherein the set of consecutively transmitted data bits are successively transferred through the circuitry in response to the first control signals.

18. The memory module of claim **15**, wherein each of the memory devices is 4-bits wide, and wherein each of the plurality of ranks is 72-bits wide and includes 18 memory devices configured in pairs, and wherein each pair of 4-bit-wide memory devices are configured to simulate an 8-bit-wide memory device.

19. The memory module of claim **15**, wherein the memory devices are organized in four ranks and the first set of input address and control signals include four chip select signals, one for each of the four ranks.

20. The memory module of claim **15**, wherein the circuitry includes logic pipelines configured to enable the data transfers between the first rank and the memory bus through the circuitry in response to the first control signals.

21. The memory module of claim **15**, wherein the logic is further configured to report the overall CAS latency to the memory controller in response to a mode register set command received from the memory controller.

22. The memory module of claim **15**, wherein the first burst of N-bit wide data signals and the first burst of data strobes are transferred between the first N-bit wide rank and the memory controller at a specified data rate.

23. The memory module of claim **15**, further comprising a phase locked loop clock driver configured to output a clock signal in response to one or more signals received from the memory controller, wherein the predetermined amount of time delay is at least one clock cycle time delay.

24. The memory module of claim **23**, wherein the memory devices are dynamic random access memory devices configured to operate synchronously with the clock signal, and wherein each memory device in the first rank is configured receive or output a respective set of bits of the first burst of N-bit wide data signals on both edges of each of a respective set of data strobes of the first burst of data strobes.

25. The memory module of claim **15**, wherein the logic is further configured to respond to a second set of input address and control signals associated with a second read or write memory command by outputting a second set of registered address and control signals, the second set of input address and control signals including a second plurality of input chip select signals, the second set of registered address and control signals including a second plurality of registered chip select signals corresponding to respective ones of the second plurality of input chip select signals, the second plurality of registered chip select signals including a second registered chip select signal having the active signal value and one or more other registered chip select signals each having the non-active signal value, wherein a second rank different from the first rank is configured to receive the second registered chip select signal having the active signal value and to output or receive a second burst of N-bit wide data signals and a second burst of data strobes associated with the second read or write command, wherein the logic is further configured to, in response to the second read or write memory command, output second control signals to the circuitry, and wherein the circuitry is configured to enable registered data transfers between the second rank and the memory bus through the circuitry in response to the second control signals so that the second burst of N-bit wide data signals and the second burst of data strobes are transferred between the second rank and the memory controller through the circuitry in accordance with the overall CAS latency of the memory module.

26. The memory module of claim **17**, wherein the first burst of N-bit wide data signals is transferred through the circuitry in a plurality of time intervals including at least a first time interval and a last time interval, wherein the circuitry includes a set of signal paths that are enabled before the first time interval and subsequently disabled after the last time interval.

27. The memory module of claim **26**, wherein:

the first read or write memory command is a read memory command;

the second read or write memory command is a write memory command;

the set of signal paths are enabled to transfer the first burst of N-bit wide data signals and the first burst of data strobes a first number of time intervals after the read memory command is received by the logic; and

the set of signal paths are enabled to transfer the second burst of N-bit wide data signals and the second burst of data strobes a second number of time intervals after the write memory command is received by the logic, the second number being different from the first number.

28. A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or

write memory commands received from the memory controller, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

logic coupled to the printed circuit board and configured to receive a set of input control and address signals associated with a read or write memory command via the memory bus and to output a set of registered control and address signals in response to the set of input control and address signals, the set of input control and address signals including a plurality of input chip select signals, the set of registered control and address signals including a plurality of registered chip select signals corresponding to respective ones of the plurality of input chip select signals, the plurality of registered chip select signals including a registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value;

memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, wherein the plurality of N-bit wide ranks are configured to receive respective ones of the plurality of registered chip select signals, wherein a first N-bit wide rank receiving the registered chip select signal having the active signal value is configured to receive or output a first burst of N-bit wide data signals and a first burst of data strobes associated with the read/write command;

circuitry between data and data strobe signal lines in the memory bus and corresponding data and data strobe pins of the memory devices, wherein the circuitry includes logic pipelines configured to enable data transfers between the first rank and the memory bus in response to the first read or write memory command, wherein respective N-bit wide data signals of the first burst of N-bit wide data signals and respective data strobes of the first burst of data strobes are transferred between the first rank and the memory bus through the circuitry in accordance with an overall CAS latency of the memory module; and

wherein the data transfers between the first rank and the memory bus are registered data transfers; and

wherein the circuitry is configured to add a predetermined amount of time delay for each data transfer between the memory controller and the memory devices such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.

29. The memory module of claim **28**, wherein the first burst of N-bit wide data signals includes a set of consecutively transmitted data bits for each data signal line in the memory bus, and wherein the circuitry includes a set of signal paths that are enabled before a first data bit of the set of consecutively transmitted data bits is transferred through the circuitry and disabled after a last data bit of the set of consecutively transmitted data bits is transferred through the circuitry.

30. The memory module of claim **28**, wherein the logic is further configured to respond to a subsequent set of input address and control signals associated with a subsequent read or write memory command by outputting a subsequent set of registered address and control signals, the subsequent set of input address and control signals including a subsequent plurality of input chip select signals, the subsequent set of registered address and control signals including a subsequent plurality of registered chip select signals corresponding to respective ones of the subsequent plurality of input chip select signals, the subsequent plurality of registered chip select signals including a subsequently registered chip select signal having the active signal value and one or more other subsequently registered chip select signals each having the non-active signal value, wherein a second rank different from the first rank is configured to receive the subsequently registered chip select signal having the active signal value and to output or receive a second burst of N-bit wide data signals and a second burst of data strobes associated with the subsequent read or write command, wherein the circuitry is further configured to enable registered data transfers between the memory devices and the memory bus in response to the subsequent read/write memory command so that the second burst of N-bit wide data signals and the second burst of data strobes are transferred between the second rank and the memory bus through the circuitry.

31. The memory module of claim **28**, wherein the first burst of N-bit wide data signals and the first burst of data strobes are transferred between the first N-bit wide rank and the memory controller at a specified data rate.

32. The memory module of claim **28**, further comprising a phase locked loop clock driver configured to output a clock signal in response to one or more signals received from the memory controller, wherein the predetermined amount of time delay is at least one clock cycle time delay.

33. The memory module of claim **32**, wherein the memory devices are dynamic random access memory devices configured to operate synchronously with the clock signal, and wherein each memory device in the first rank is configured receive or output a respective set of bits of the first burst of N-bit wide data signals on both edges of each of a respective set of data strobes of the first burst of data strobes.

* * * * *

CERTIFICATE OF SERVICE

I certify that on June 26, 2024, the foregoing brief was filed with the Clerk of Court and caused to be served on all parties through the Court's electronic filing system. I further certify that all parties required to be served have been served.

/s/ Michael R. Rueckheim
Michael R. Rueckheim
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June 26, 2024

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